1 Mbit / 2 Mbit (x8) Multi-Purpose Flash
SST39SF010A / SST39SF020A

Data Sheet

FEATURES:

- **Organized as 128K x8 / 256K x8**
- **Single 5.0V Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 10 mA (typical)
  - Standby Current: 30 µA (typical)
- **Sector-Erase Capability**
  - Uniform 4 KByte sectors
- **Fast Read Access Time:**
  - 45 and 70 ns
- **Latched Address and Data**
- **Fast Erase and Byte-Program:**
  - Sector-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 70 ms (typical)
  - Byte-Program Time: 14 µs (typical)
  - Chip Rewrite Time:
    2 seconds (typical) for SST39SF010A
    4 seconds (typical) for SST39SF020A
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **TTL I/O Compatibility**
- **JEDEC Standard**
  - Flash EEPROM Pinouts and command sets
- **Packages Available**
  - 32-Pin PDIP
  - 32-Pin PLCC
  - 32-Pin TSOP (8mm x 14mm)

PRODUCT DESCRIPTION

The SST39SF010A/020A are CMOS Multi-Purpose Flash (MPF) manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39SF010A/020A devices write (Program or Erase) with a 5.0V power supply. The SST39SF010A/020A device conforms to JEDEC standard pinouts for x8 memories.

Featuring high performance Byte-Program, the SST39SF010A/020A devices provide a maximum Byte-Program time of 20 µsec. These devices use Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, they have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST39SF010A/020A devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, they significantly improve performance and reliability, while lowering power consumption. They inherently use less energy during erase and program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. These devices also improve flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high density, surface mount requirements, the SST39SF010A/020A are offered in 32-pin TSOP and 32-pin PLCC packages. A 600 mil, 32-pin PDIP is also available. See Figures 1, 2 and 3 for pinouts.

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Read

The Read operation of the SST39SF010A/020A is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to Figure 4 for the Read cycle timing diagram.

Byte-Program Operation

The SST39SF010A/020A are programmed on a byte-by-byte basis. The Program operation consists of three steps. The first step is the three-byte-load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed, within 20 µs. See Figures 5 and 6 for WE# and CE# controlled Program operation timing diagrams and Figure 15 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Sector-Erase Operation

The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte-command load sequence for Software Data Protection with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The sector address is latched on the falling edge of the sixth WE# pulse , while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 9 for timing waveforms. Any commands written during the Sector-Erase operation will be ignored.

Chip-Erase Operation

The SST39SF010A/020A provide Chip-Erase operation, which allows the user to erase the entire memory array to the "1's" state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip-Erase command (10H) with address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 10 for timing diagram, and Figure 18 for the flowchart. Any commands written during the Chip-Erase operation will be ignored.

Write Operation Status Detection

The SST39SF010A/020A provide two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the program or erase cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the SST39SF010A/020A are in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. The device is then ready for the next operation. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program Operation. For Sector- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e., toggling between 0 and 1. The Toggle Bit will begin with "1". When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising

edge of fourth WE# (or CE#) pulse for Program operation. For Sector- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 8 for Toggle Bit timing diagram and Figure 16 for a flowchart.

Data Protection

The SST39SF010A/020A provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The write operation is inhibited when V_{DD} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST39SF010A/020A provide the JEDEC approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three byte sequence. The three byte-load sequence is used to initiate the Program operation, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six byte load sequence. The SST39SF010A/020A devices are shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode, within T_{RC}.

Product Identification

The product identification mode identifies the device as the SST39SF010A and SST39SF020A and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the SST39SF010A/020A. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 17 for the ID entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	0000H	BF H
Device ID		
SST39SF010A	0001H	B5 H
SST39SF020A	0001H	B6 H

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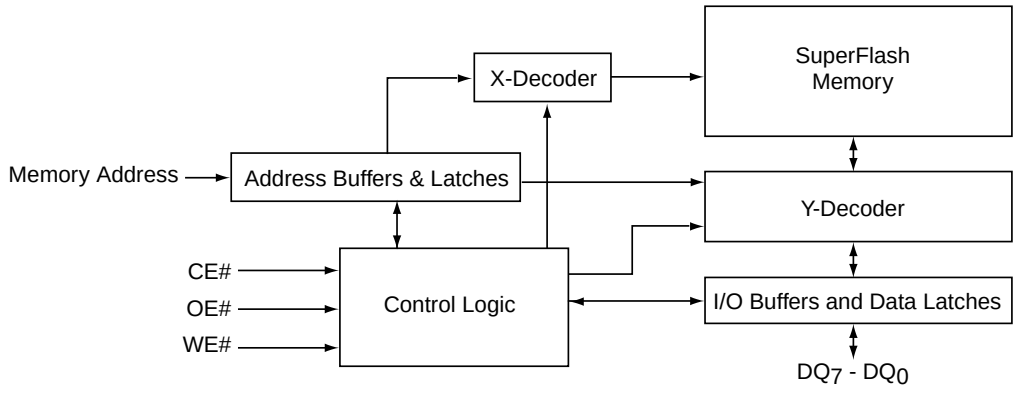
Product Identification Mode Exit/Reset

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Exit ID command sequence, which returns the device to the Read operation. Please note that the software reset command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 12 for timing waveform and Figure 17 for a flowchart.

FUNCTIONAL BLOCK DIAGRAM



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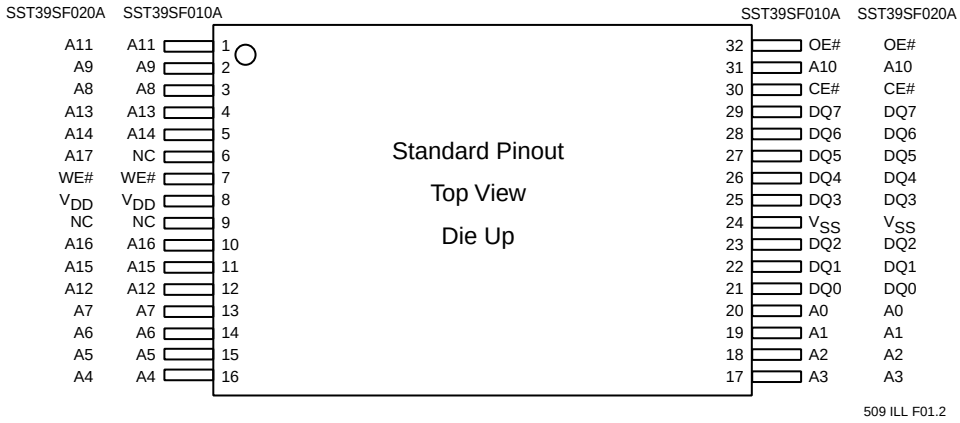

FIGURE 1: PIN ASSIGNMENTS FOR 32-PIN TSOP (8mm x 14mm)

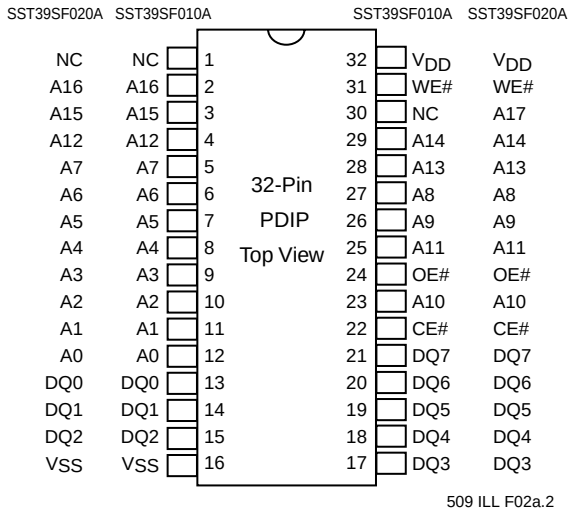

FIGURE 2: PIN ASSIGNMENTS FOR 32-PIN PDIP

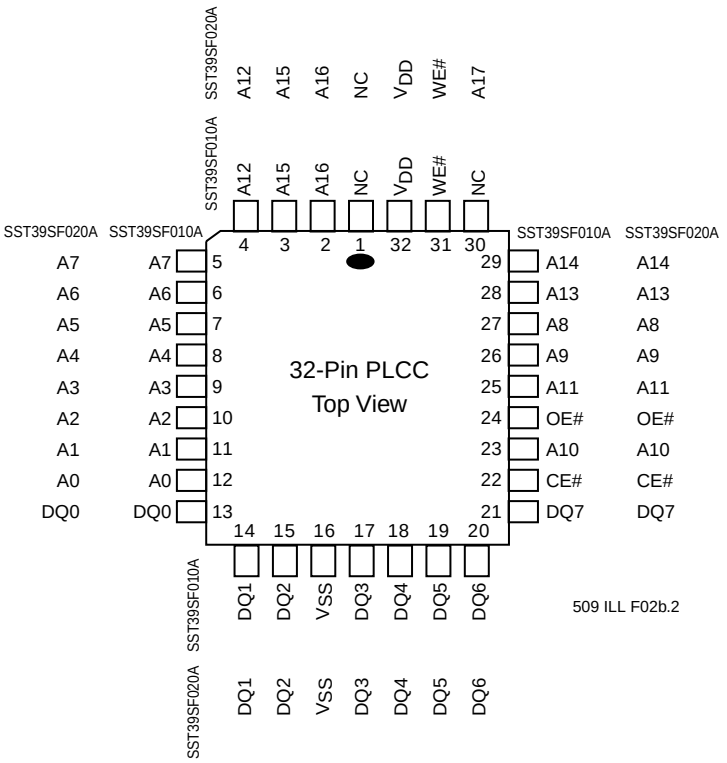

FIGURE 3: PIN ASSIGNMENTS FOR 32-PIN PLCC

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{MS}-A_0	Address Inputs	To provide memory addresses. During Sector-Erase A_{MS}-A_{12} address lines will select the sector.
DQ_7-DQ_0	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the Write operations.
V_{DD}	Power Supply	To provide 5-volt supply (± 10%)
V_{SS}	Ground	
NC	No Connection	Unconnected pins.

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Note: A_{MS} = Most significant address
A_{MS} = A_{16} for SST39SF010A and A_{17} for SST39SF020A

TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	A9	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}	A_{IN}
Program	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}	A_{IN}
Erase	V_{IL}	V_{IH}	V_{IL}	X	X	Sector address, XXH for Chip-Erase
Standby	V_{IH}	X	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	X	High Z/D_{OUT}	X
	X	X	V_{IH}	X	High Z/D_{OUT}	X
Product Identification Hardware Mode	V_{IL}	V_{IL}	V_{IH}	V_H	Manufacturer's ID (BFH) Device ID[1]	A_{MS}[2] - A_1 = V_{IL}, A_0 = V_{IL} A_{MS}[2] - A_1 = V_{IL}, A_0 = V_{IH}
Software Mode	V_{IL}	V_{IL}	V_{IH}	A_{IN}	ID Code	See Table 4

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Note: 1. Device ID = B5H for SST39SF010A and B6H for SST39SF020A
2. A_{MS} = Most significant address
A_{MS} = A_{16} for SST39SF010A and A_{17} for SST39SF020A

TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Byte-Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA[3]	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA_X[2]	30H
Chip-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	XXH	F0H										
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

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Notes:

1. Address format A_{14}-A_0 (Hex), Address A_{16} and A_{15} are "Don't Care" for the Command sequence for SST39SF010A.
   Address A_{15}, A_{16} and A_{17} are "Don't Care" for the Command sequence for SST39SF020A.
2. SA_X for Sector-Erase; uses A_{MS}-A_{12} address lines
   A_{MS} = Most significant address
   A_{MS} = A_{16} for SST39SF010A and A_{17} for SST39SF020A
3. BA = Program Byte address
4. Both Software ID Exit operations are equivalent
5. With A_{MS} -A_1 =0; SST Manufacturer's ID = BFH, is read with A_0 = 0,
   SST39SF010A Device ID = B5 H, is read with A_0 = 1.
   SST39SF020A Device ID = B6 H, is read with A_0 = 1.
6. The device does not remain in Software Product ID Mode if powered down.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{DD}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{DD}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 13.2V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 50 mA

Note: 1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0 °C to +70 °C	5V±10%
Industrial	-40 °C to +85 °C	5V±10%

AC CONDITIONS OF TEST

Input Rise/Fall Time ..... 5 ns
Output Load ..... C_L = 30 pF
See Figures 13 and 14

TABLE 5: DC OPERATING CHARACTERISTICS V_{DD} = 5V±10%

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current				Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., $V_{DD}=V_{DD}$ Max
	Read		20	mA	CE#=OE#=V_{IL},WE#=V_{IH} , all I/Os open.
	Write		20	mA	CE#=WE#=V_{IL}, OE#=V_{IH}
I_{SB1}	Standby V_{DD} Current (TTL input)		3	mA	CE#=V_{IH}, V_{DD} =V_{DD} Max.
I_{SB2}	Standby V_{DD} Current (CMOS input)		100	µA	CE#=V_{IHC}. V_{DD} = V_{DD} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{DD}, V_{DD} = V_{DD} Max.
I_{LO}	Output Leakage Current		1	µA	V_{OUT} =GND to V_{DD}, V_{DD} = V_{DD} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{DD} = V_{DD} Min.
V_{IH}	Input High Voltage	2.0		V	V_{DD} = V_{DD} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA, V_{DD} = V_{DD} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA, V_{DD} = V_{DD} Min.
V_H	Supervoltage for A_9 pin	11.4	12.6	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9 pin		200	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

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TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

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TABLE 7: CAPACITANCE (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

509 PGM T7.0

Note: (1)This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	2000	Volts	JEDEC Standard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

509 PGM T8.1

Note: 1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 9: READ CYCLE TIMING PARAMETERS V_{DD} = 4.5-5.5V

		SST39SF010A/020A-45		SST39SF010A/020A-70		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
T_{RC}	Read Cycle Time	45		70		ns
T_{CE}	Chip Enable Access Time		45		70	ns
T_{AA}	Address Access Time		45		70	ns
T_{OE}	Output Enable Access Time		25		35	ns
T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{CHZ}[1]	CE# High to High-Z Output		15		25	ns
T_{OHZ}[1]	OE# High to High-Z Output		15		25	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns

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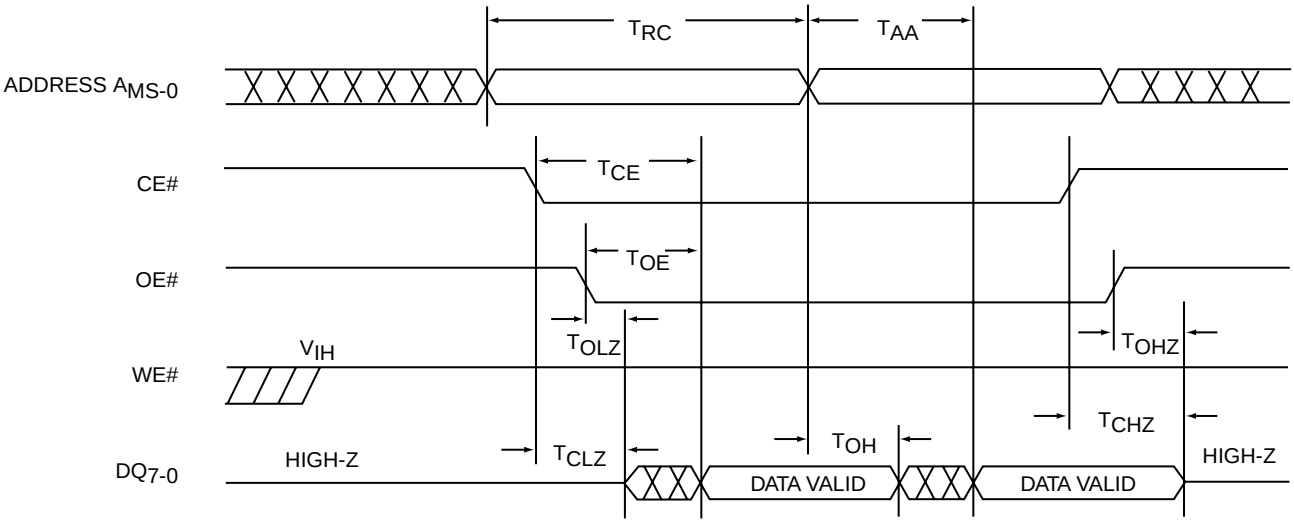
TABLE 10: PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	**Parameter**	**Min**	**Max**	**Units**
T_{BP}	Byte-Program Time		20	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	30		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{CP}	CE# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}[1]	WE# Pulse Width High	30		ns
T_{CPH}[1]	CE# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH}[1]	Data Hold Time	0		ns
T_{IDA}[1]	Software ID Access and Exit Time		150	ns
T_{SE}	Sector-Erase		25	ms
T_{SCE}	Chip-Erase		100	ms

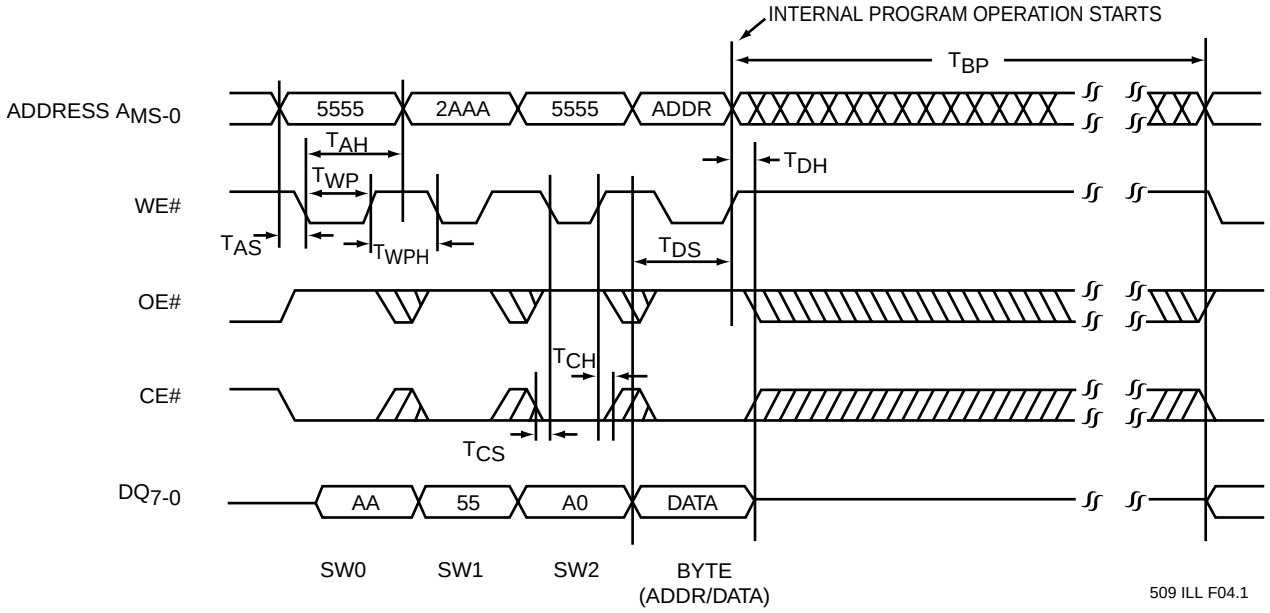
509 PGM T10.1

Note: 1. This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.



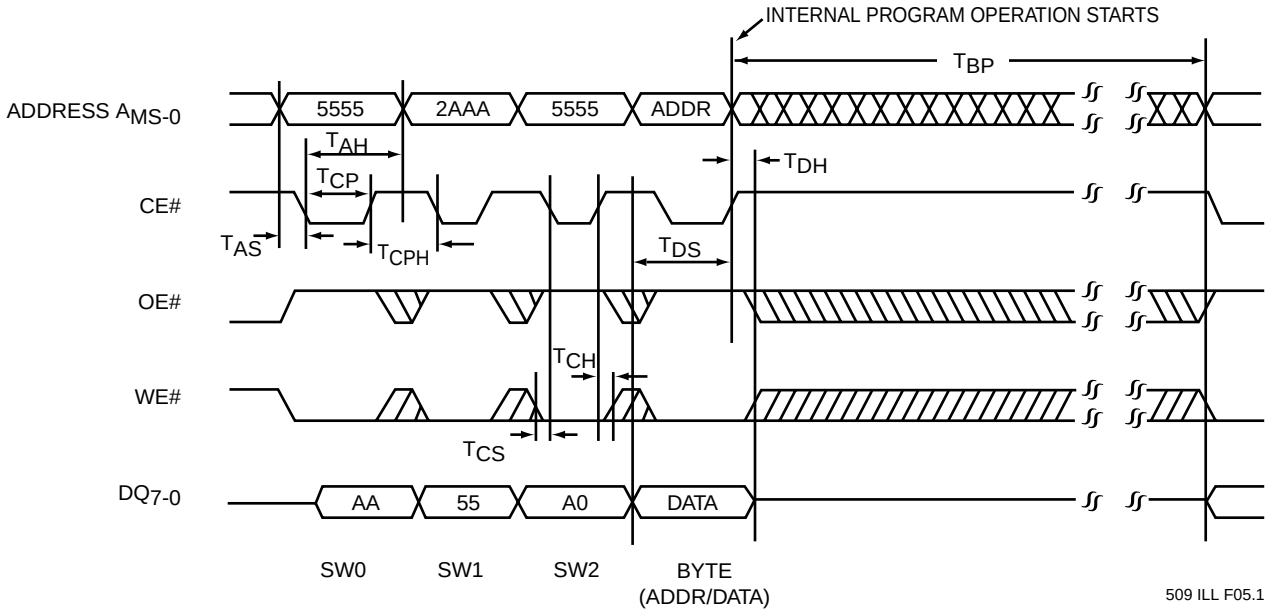
Note: A_{MS} = Most significant address
$A_{MS} = A_{16}$ for SST39SF010A and A_{17} for SST39SF020A

FIGURE 4: READ CYCLE TIMING DIAGRAM



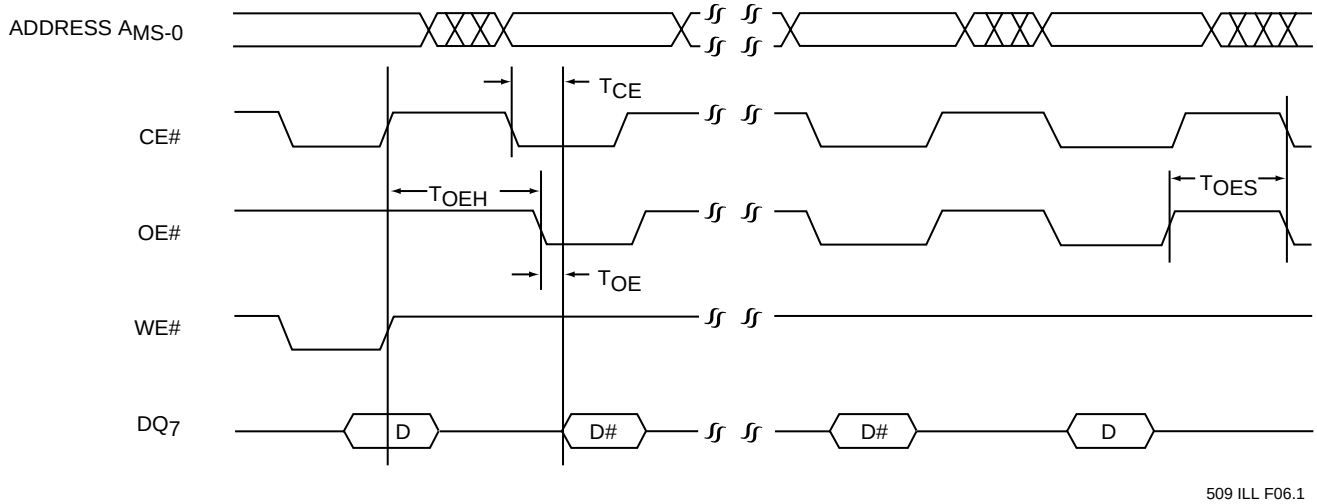
Note: A_{MS} = Most significant address
$A_{MS} = A_{16}$ for SST39SF010A and A_{17} for SST39SF020A

FIGURE 5: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



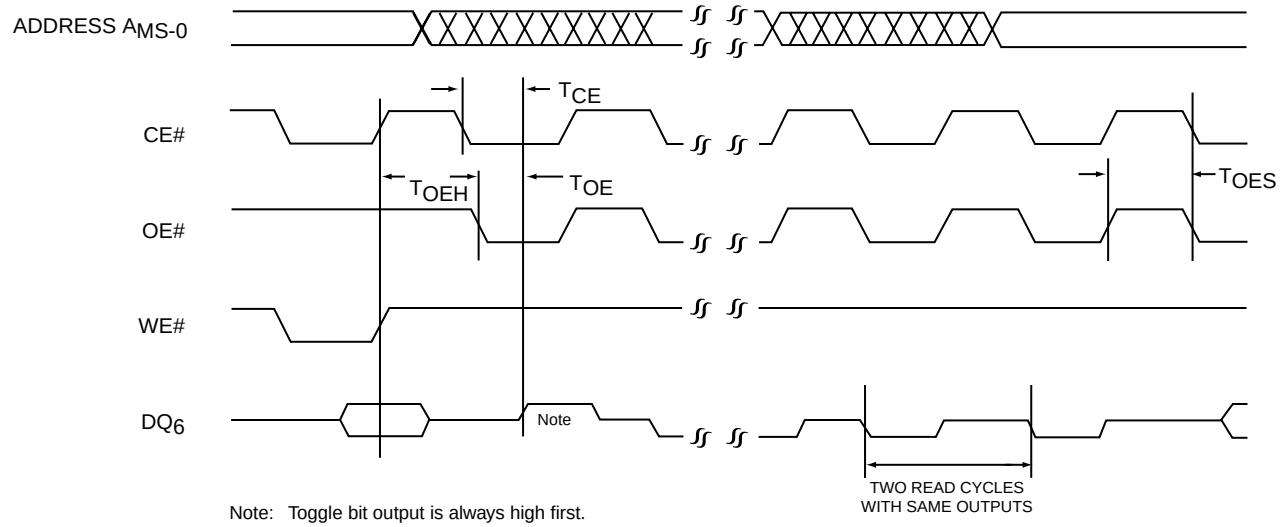
Note: A_{MS} = Most significant address
$A_{MS} = A_{16}$ for SST39SF010A and A_{17} for SST39SF020A

FIGURE 6: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



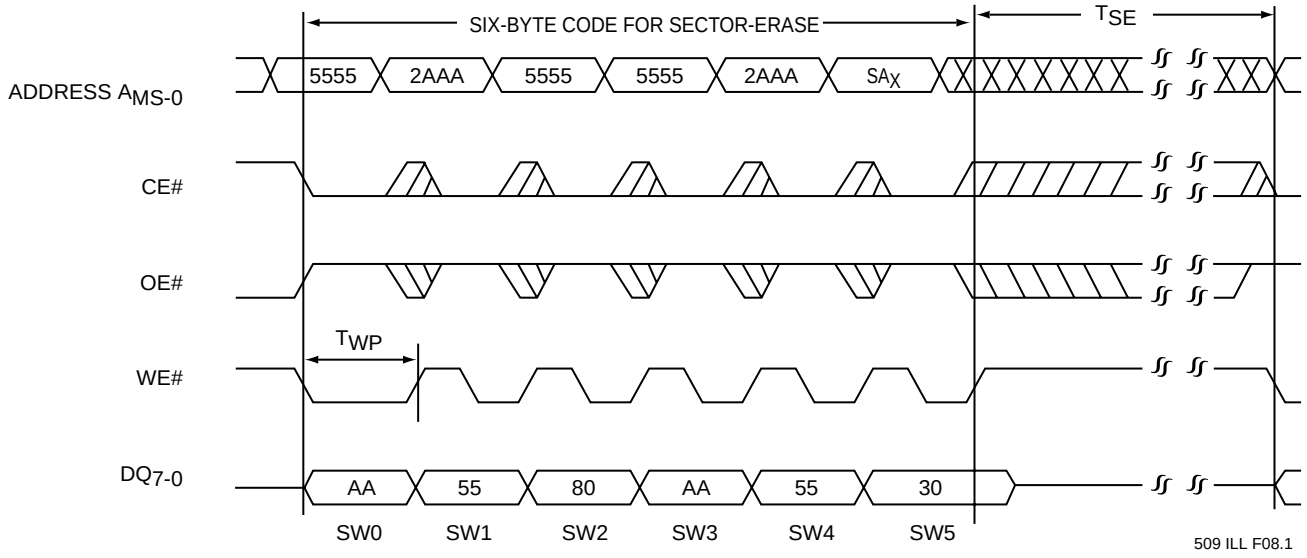
Note: A_{MS} = Most significant address
$A_{MS} = A_{16}$ for SST39SF010A and A_{17} for SST39SF020A

FIGURE 7: DATA# POLLING TIMING DIAGRAM



Note: Toggle bit output is always high first.
A_{MS} = Most significant address
A_{MS} = A_{16} for SST39SF010A and A_{17} for SST39SF020A

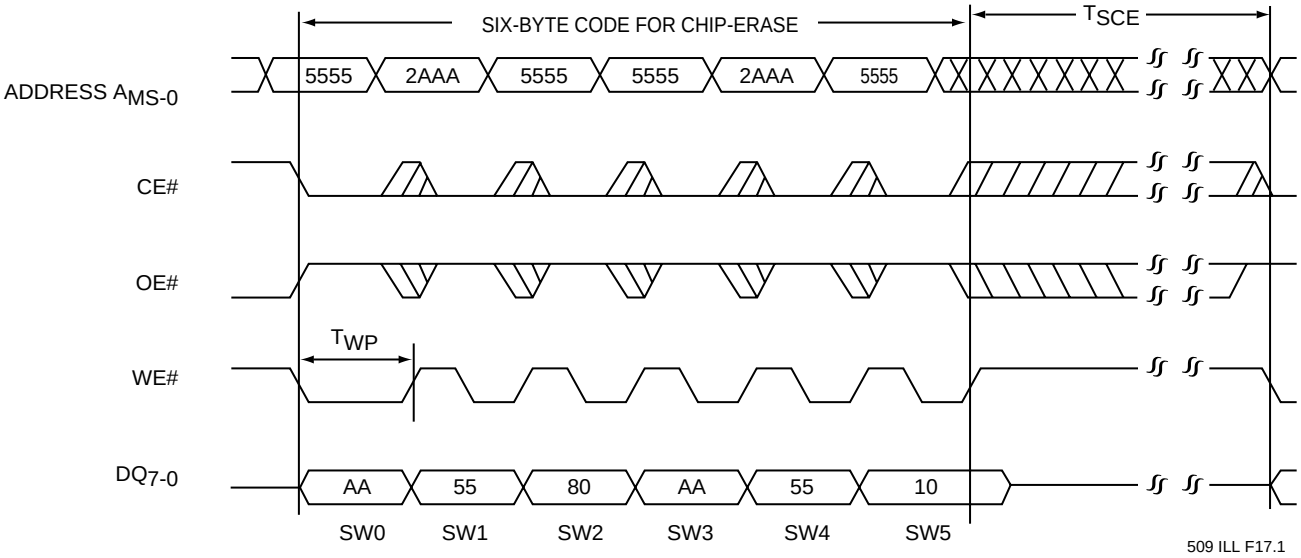
FIGURE 8: TOGGLE BIT TIMING DIAGRAM



Note: This device also supports CE# controlled Sector-Erase operation. The WE# and CE# signals are interchageable as long as minimum timings are met. (See Table 10)
SA_X = Sector Address

A_{MS} = Most significant address
A_{MS} = A_{16} for SST39SF010A and A_{17} for SST39SF020A

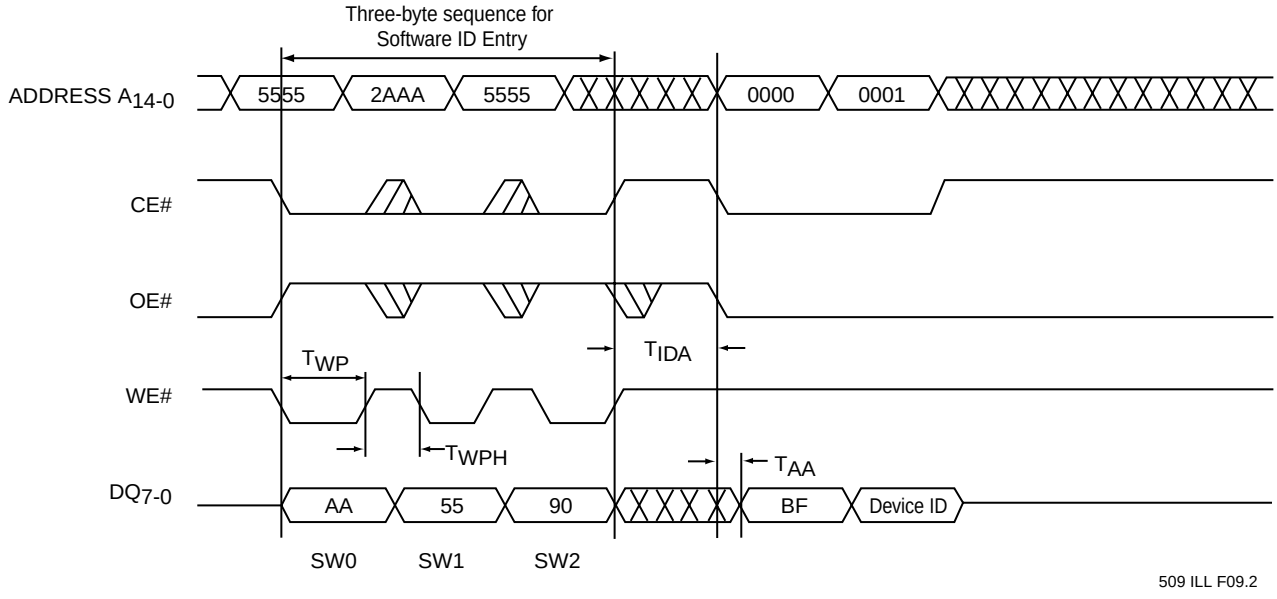
FIGURE 9: WE# CONTROLLED SECTOR-ERASE TIMING DIAGRAM



Note: This device also supports CE# controlled Chip-Erase operation. The WE# and CE# signals are interchageable as long as minimum timings are met. (See Table 10)
SA_X = Sector Address

A_{MS} = Most significant address
A_{MS} = A_{16} for SST39SF010A and A_{17} for SST39SF020A

FIGURE 10: WE# CONTROLLED CHIP-ERASE TIMING DIAGRAM



Device ID = B5H for SST39SF010A and B6H for SST39SF020A

FIGURE 11: SOFTWARE ID ENTRY AND READ

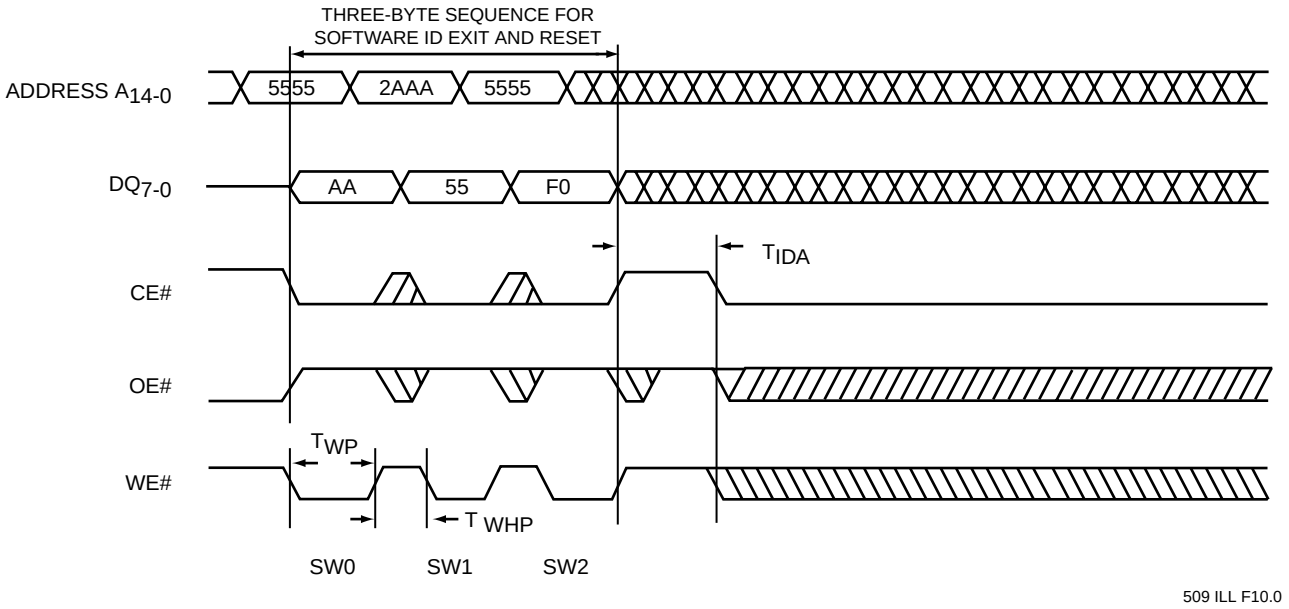
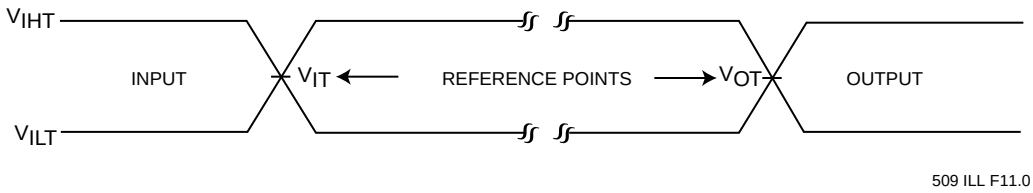


FIGURE 12: SOFTWARE ID EXIT AND RESET



AC test inputs are driven at V_{IHT} (3.0 V) for a logic "1" and V_{ILT} (0 V) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (1.5 V) and V_{OT} (1.5 V). Inputs rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT}–V_{INPUT} Test
V_{OT}–V_{OUTPUT} Test
V_{IHT}–V_{INPUT} HIGH Test
V_{ILT}–V_{INPUT} LOW Test

FIGURE 13: AC INPUT/OUTPUT REFERENCE WAVEFORMS

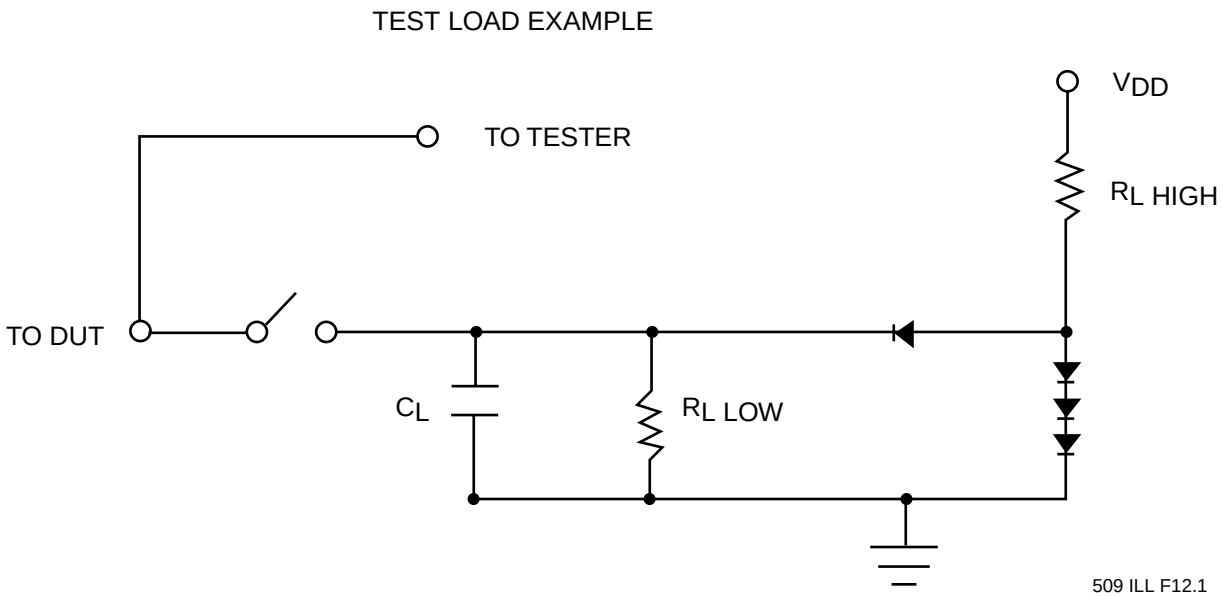


FIGURE 14: A TEST LOAD EXAMPLE

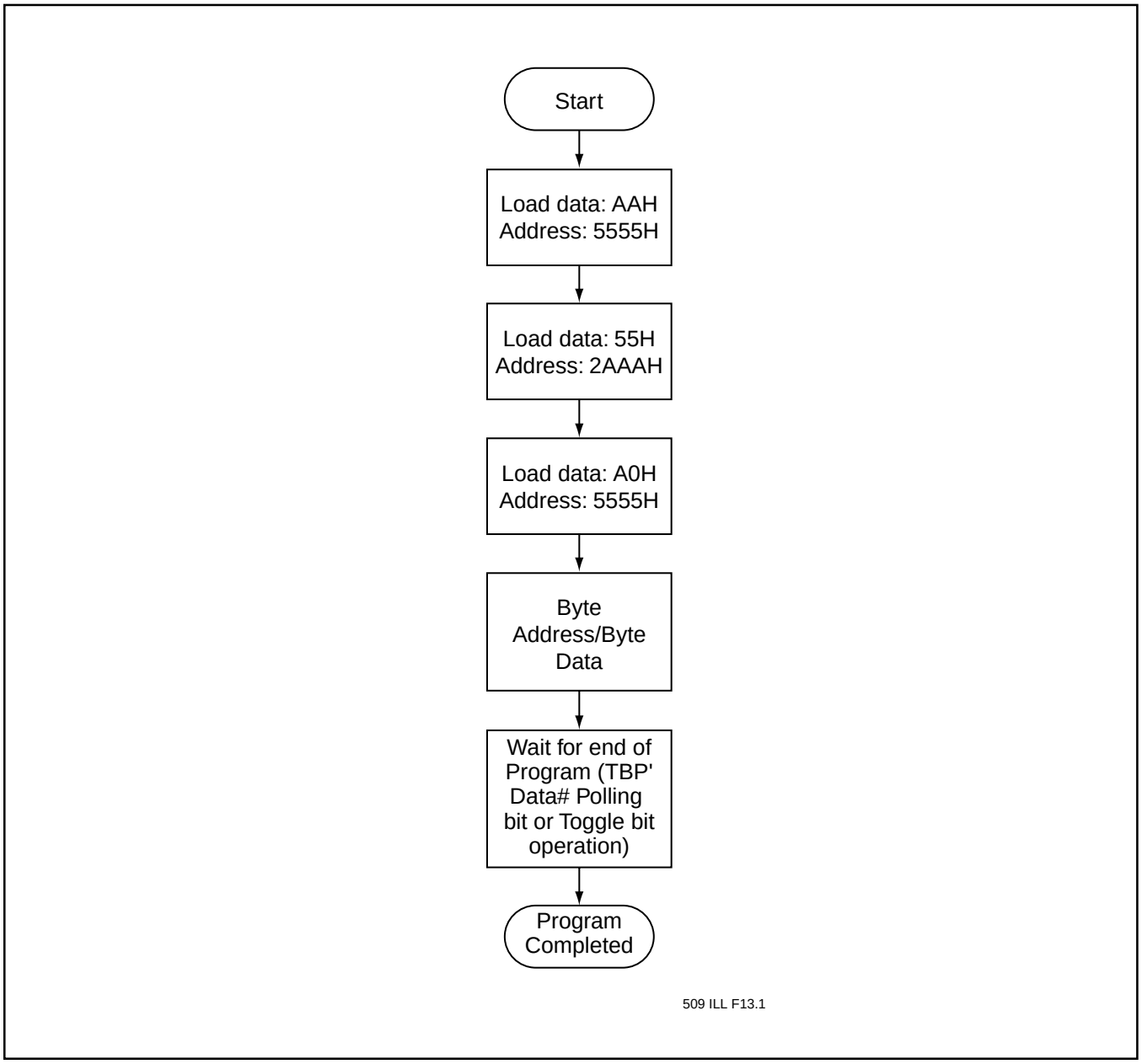


FIGURE 15: BYTE-PROGRAM ALGORITHM

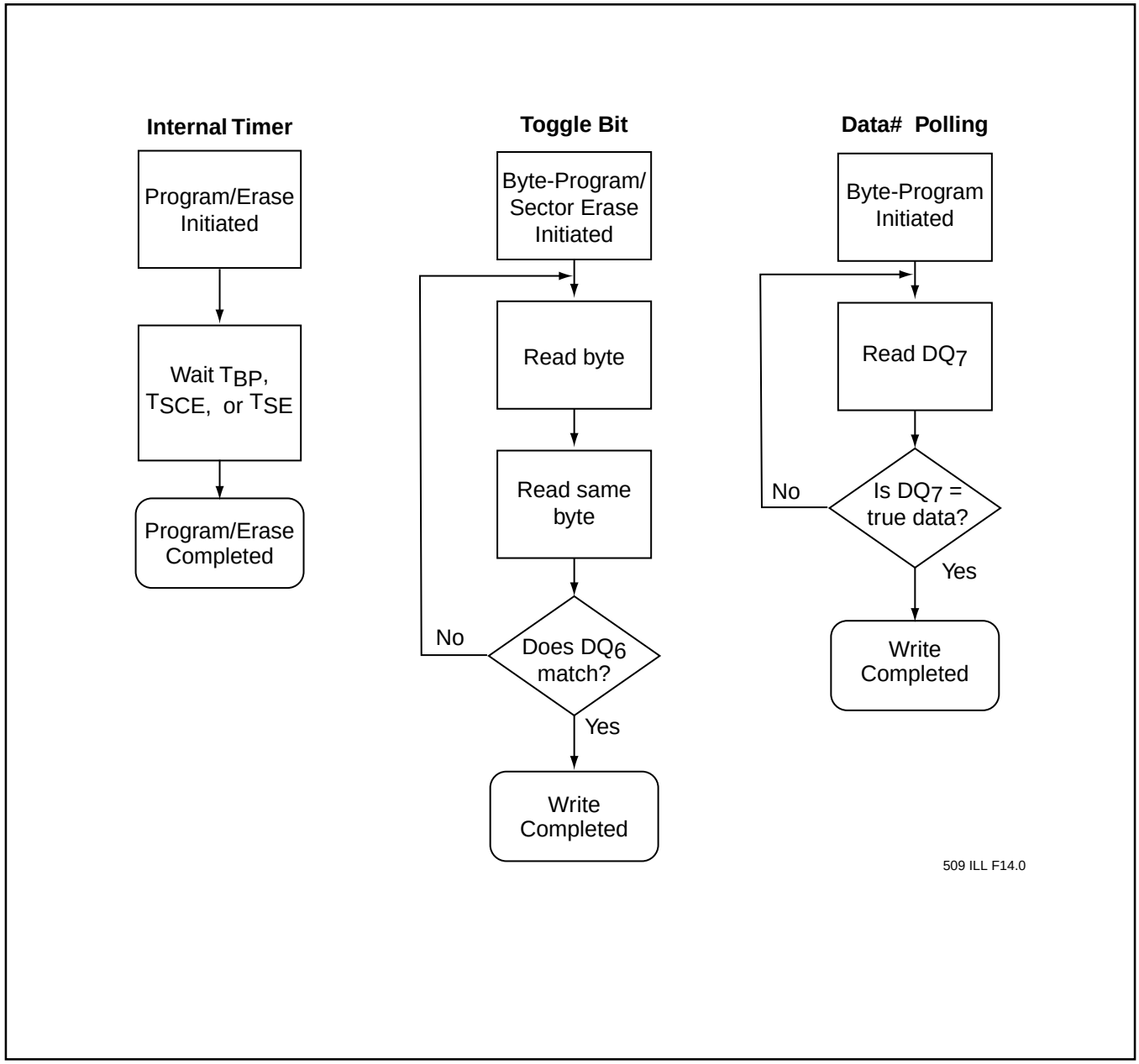


FIGURE 16: WAIT OPTIONS

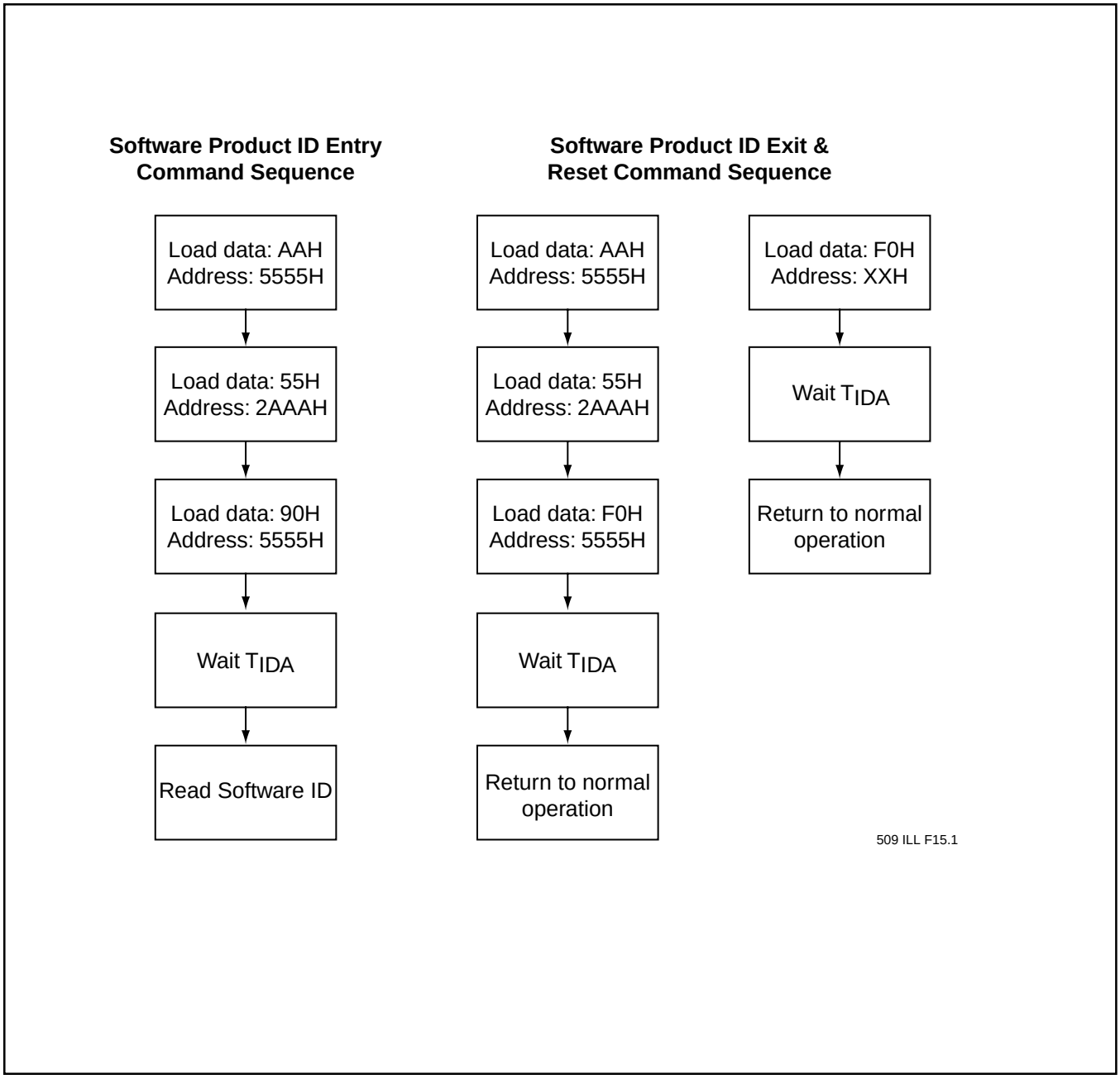


FIGURE 17: SOFTWARE PRODUCT COMMAND FLOWCHARTS

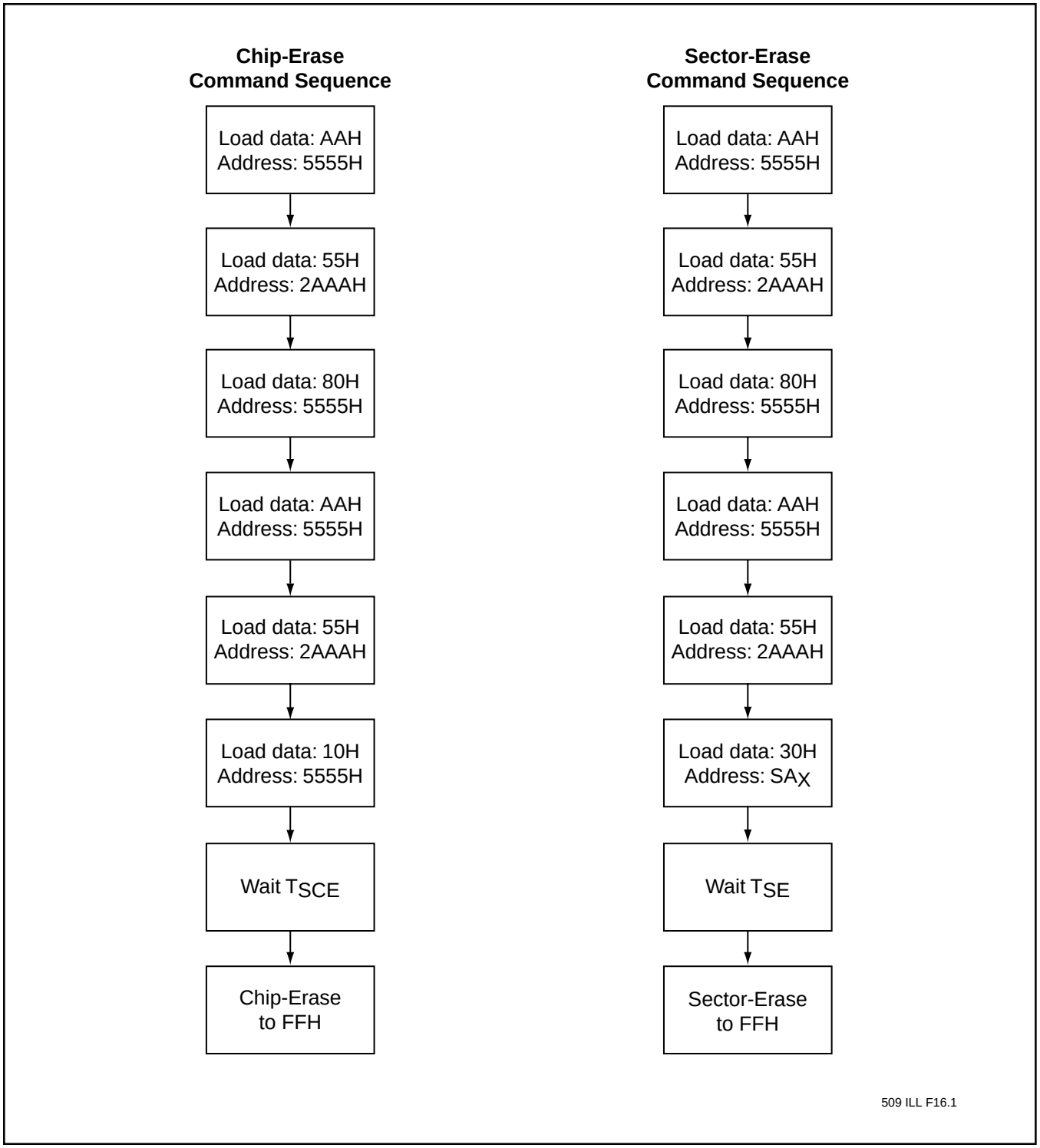
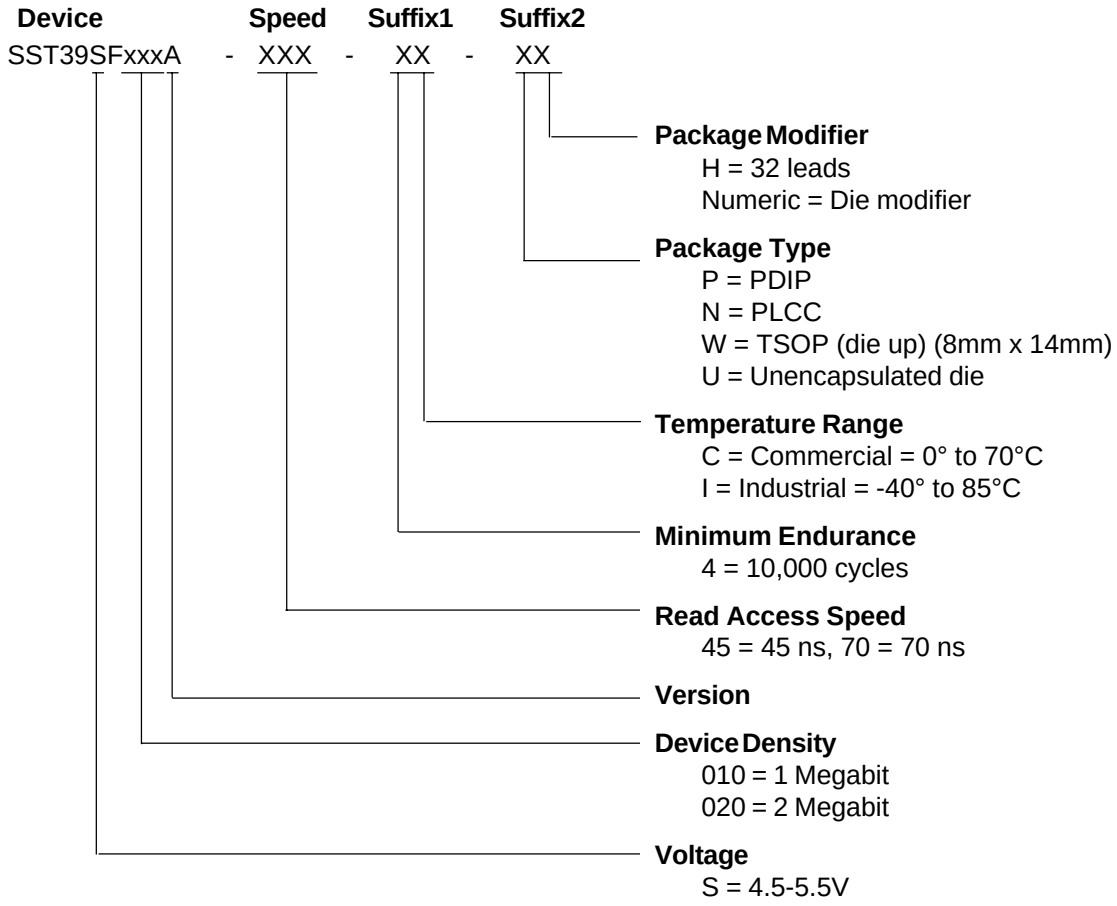


FIGURE 18: ERASE COMMAND SEQUENCE



SST39SF010A Valid combinations

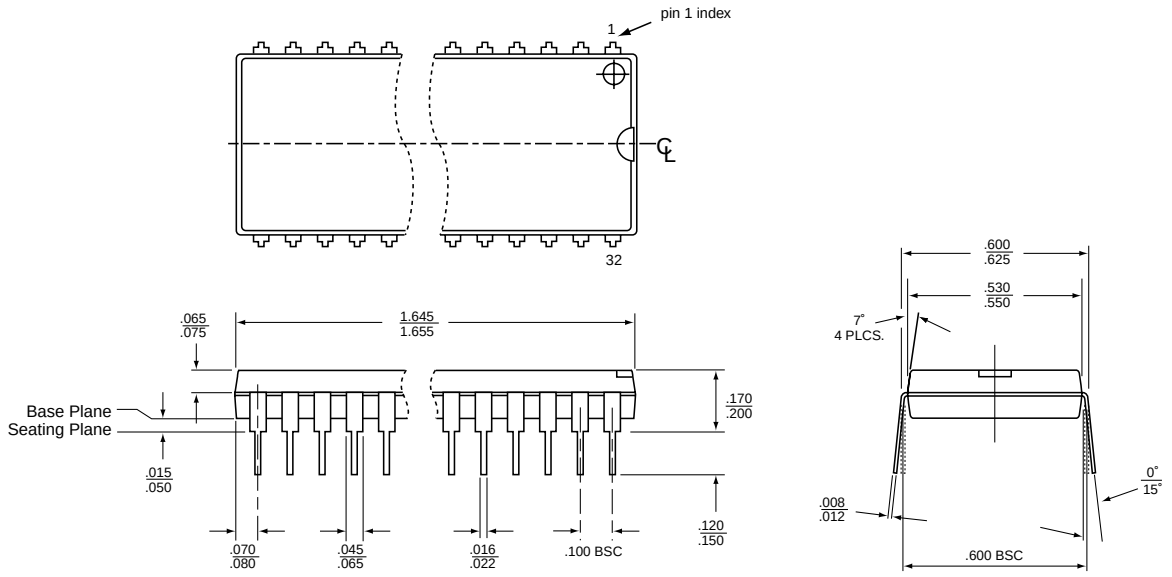
SST39SF010A-45-4C-WH	SST39SF010A-45-4C-NH	
SST39SF010A-70-4C-WH	SST39SF010A-70-4C-NH	SST39SF010A-70-4C-PH
SST39SF010A-70-4C-U1		
SST39SF010A-45-4I-WH	SST39SF010A-45-4I-NH	
SST39SF010A-70-4I-WH	SST39SF010A-70-4I-NH	

SST39SF020A Valid combinations

SST39SF020A-45-4C-WH	SST39SF020A-45-4C-NH	
SST39SF020A-70-4C-WH	SST39SF020A-70-4C-NH	SST39SF020A-70-4C-PH
SST39SF020A-70-4C-U1		
SST39SF020A-45-4I-WH	SST39SF020A-45-4I-NH	
SST39SF020A-70-4I-WH	SST39SF020A-70-4I-NH	

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

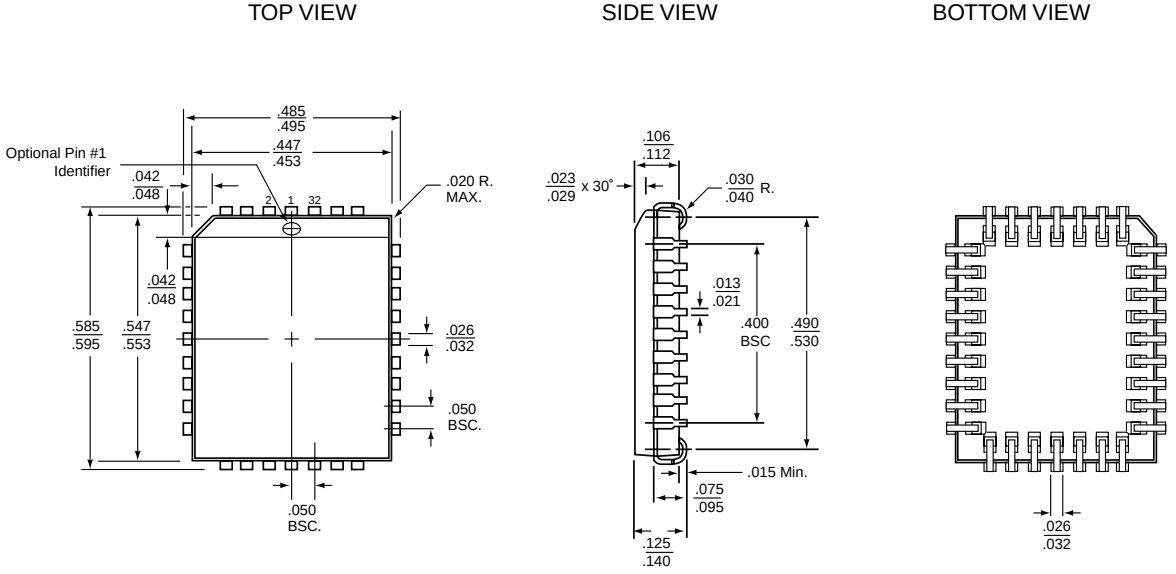
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MO-015 AP dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

32.pdipPH-ILL.1

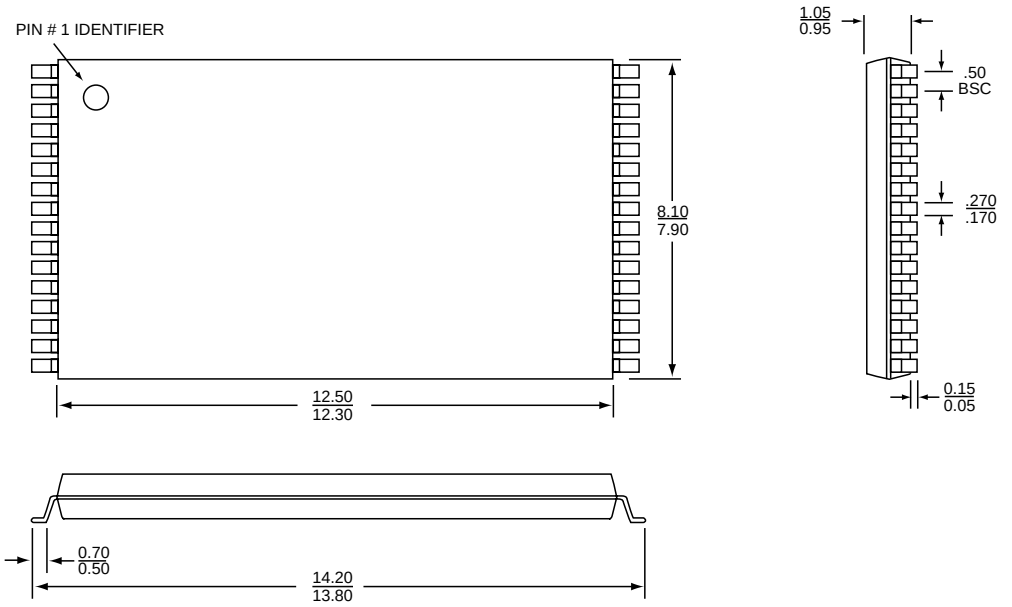
32-PIN PLASTIC DUAL-IN-LINE PACKAGE (PDIP)
SST PACKAGE CODE: PH



Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.

32.PLCC.NH-ILL.1

32-PIN PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH



Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (min/max).
3. Coplanarity: 0.1 (±.05) mm.

32.TSOP-WH-ILL.3

32-PIN THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM
SST PACKAGE CODE: WH