



M58LW064D

64 Mbit (8Mb x8, 4Mb x16, Uniform Block)
3V Supply Flash Memory

FEATURES SUMMARY

- WIDE x8 or x16 DATA BUS for HIGH BANDWIDTH
- SUPPLY VOLTAGE
 - $V_{DD} = V_{DDQ} = 2.7$ to $3.6V$ for Program, Erase and Read operations
- ACCESS TIME
 - Random Read 110ns
 - Page Mode Read 110/25ns
- PROGRAMMING TIME
 - 16 Word Write Buffer
 - $12\mu s$ Word effective programming time
- 64 UNIFORM 64 KWord/128KByte MEMORY BLOCKS
- ENHANCED SECURITY
 - Block Protection/ Unprotection
 - V_{PEN} signal for Program Erase Enable
 - 128 bit Protection Register with 64 bit Unique Code in OTP area
- PROGRAM and ERASE SUSPEND
- COMMON FLASH INTERFACE
- 100, 000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
 - Manufacturer Code: 0020h
 - Device Code M58LW064D: 0017h
- PACKAGES
 - Compliant with Lead-Free Soldering Processes
 - Lead-Free Versions

Figure 1. Packages

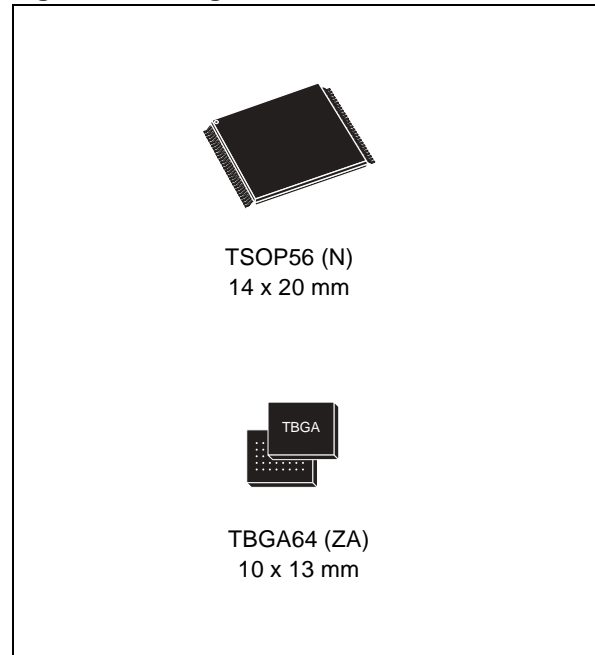


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SUMMARY DESCRIPTION

The M58LW064D is a 64 Mbit (8Mb x 8 or 4Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7V to 3.6V) core supply.

The memory is divided into 64 blocks of 1Mbit that can be erased independently so it is possible to preserve valid data while old data is erased. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a Program or Erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

The Write Buffer allows the microprocessor to program from 1 to 16 Words in parallel, both speeding up the programming and freeing up the microprocessor to perform other work. A Word Program command is available to program a single word.

Erase can be suspended in order to perform either Read or Program in any other block and then resumed. Program can be suspended to Read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

The M58LW064D has several security features to increase data protection.

- Block Protection, where each block can be individually protected against program or erase operations. All blocks are protected during power-up. The protection of the blocks is non-volatile; after power-up the protection status of each block is restored to the state when power was last removed.

- Program Erase Enable input V_{PEN} , program or erase operations are not possible when the Program Erase Enable input V_{PEN} is low.
- 128 bit Protection Register, divided into two 64 bit segments: the first contains a unique device number written by ST, the second is user programmable. The user programmable segment can be protected.

The Reset/Power-Down pin is used to apply a Hardware Reset to the enabled memory and to set the device in power-down mode.

The device features an Auto Low Power mode. If the bus becomes inactive during read operations, the device automatically enters Auto Low Power mode. In this mode the power consumption is reduced to the Auto Low Power supply current.

The STS signal is an open drain output that can be used to identify the Program/Erase Controller status. It can be configured in two modes: Ready/Busy mode where a static signal indicates the status of the P/E.C, and Status mode where a pulsing signal indicates the end of a Program or Block Erase operation. In Status mode it can be used as a system interrupt signal, useful for saving CPU time.

The memory is available in TSOP56 (14 x 20 mm) and TBGA64 (10x13mm, 1mm pitch) packages.

In addition to the standard version, the packages are also available in Lead-free version, in compliance with JEDEC Std J-STD-020B, the ST ECO-PACK 7191395 Specification, and the RoHS (Restriction of Hazardous Substances) directive.

All packages are compliant with Lead-free soldering processes.

M58LW064D

Figure 2. Logic Diagram

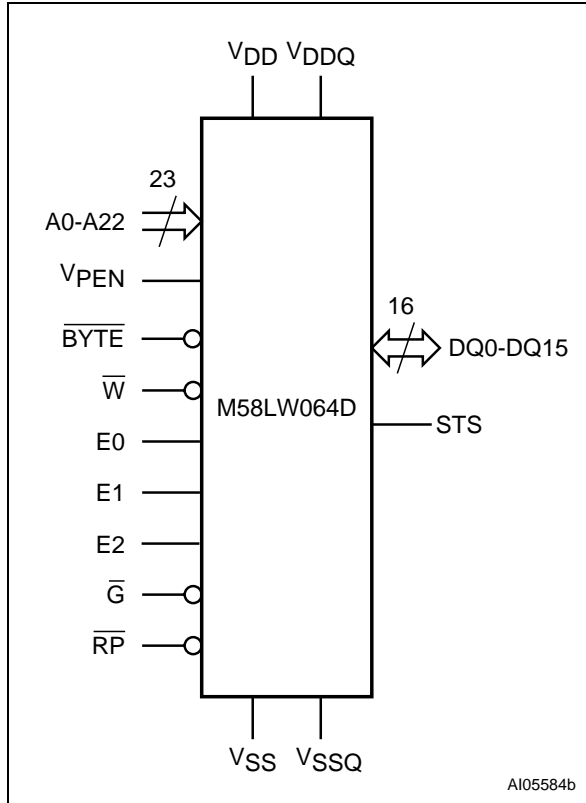
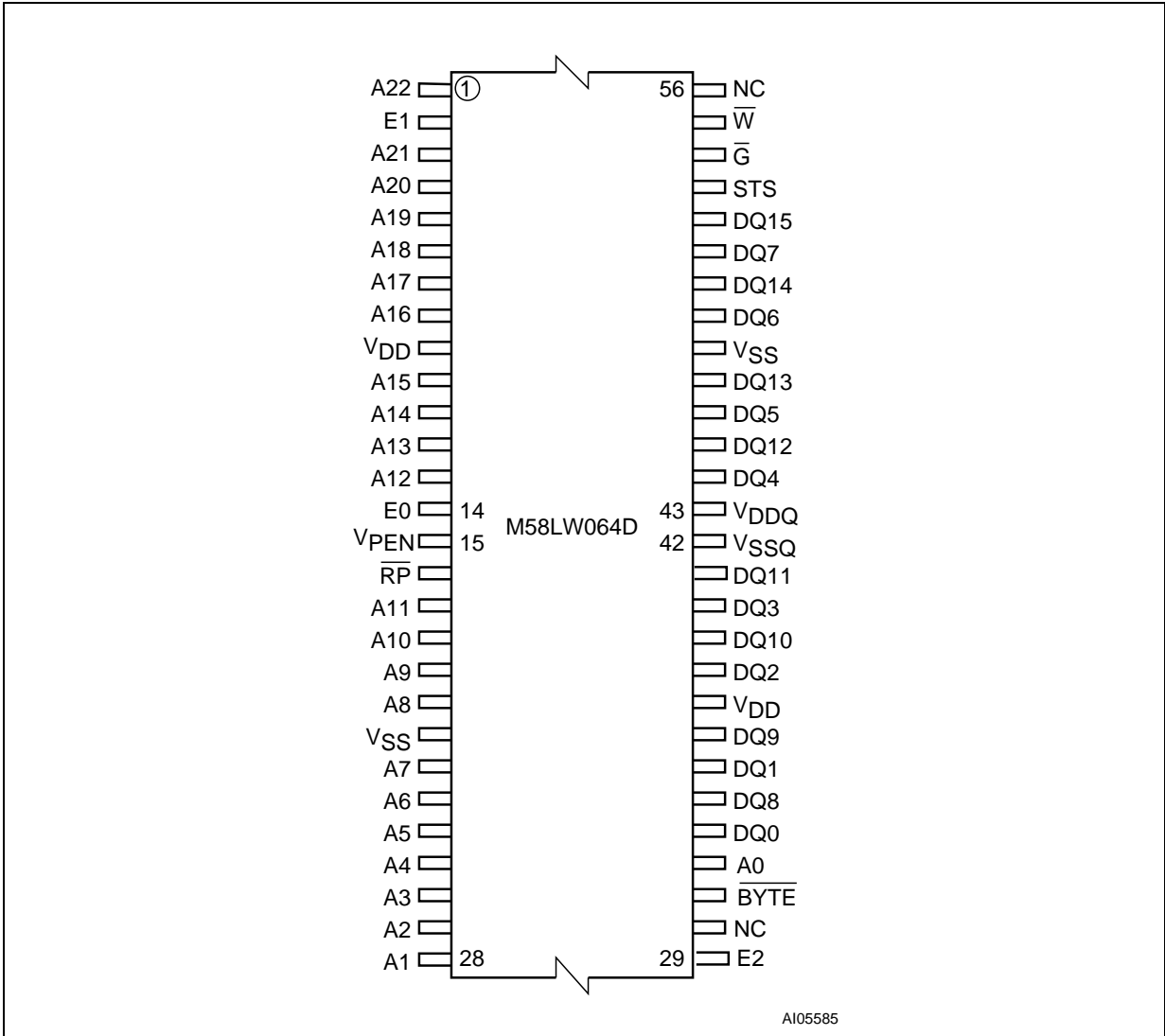


Table 1. Signal Names

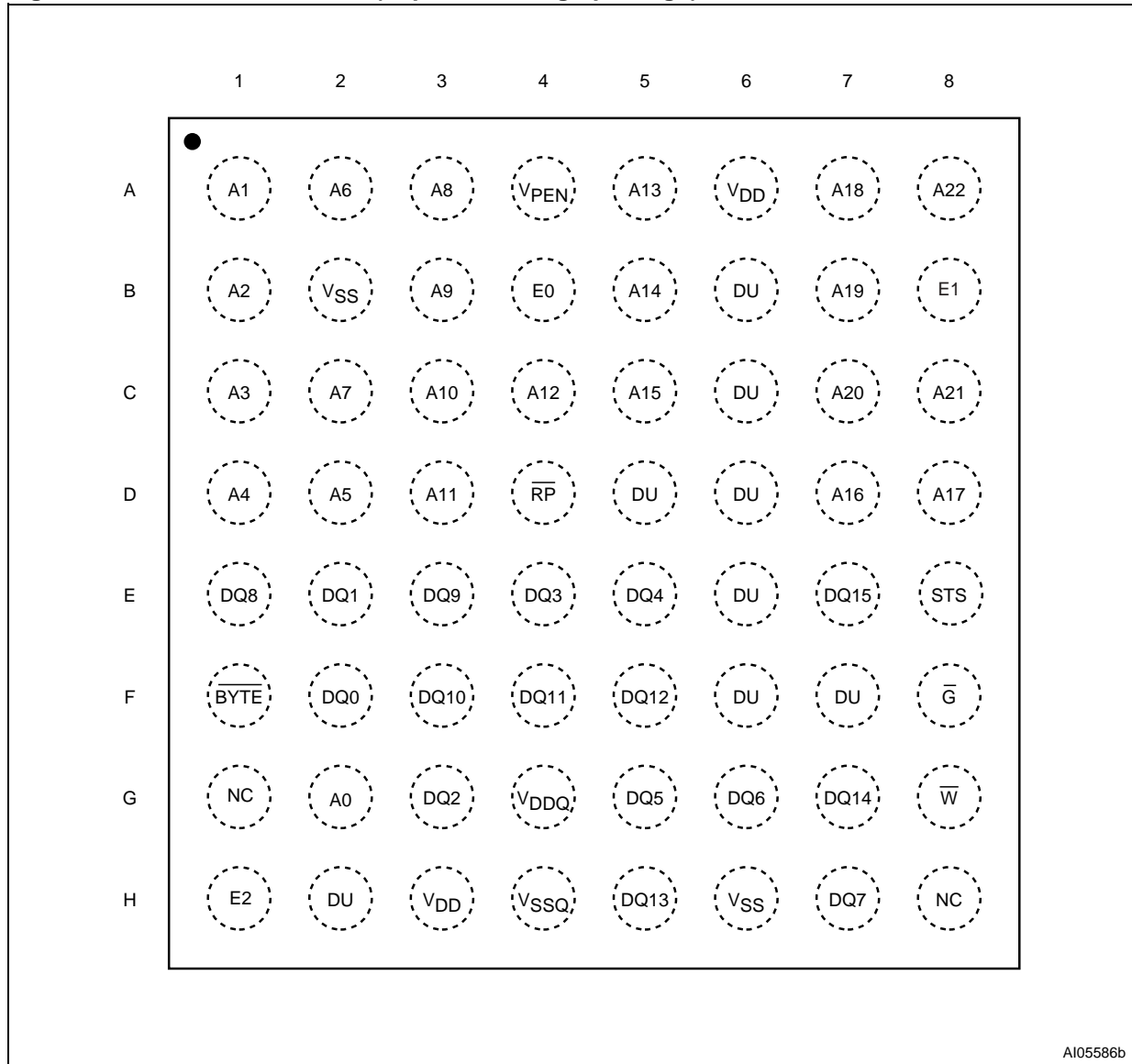
| | |
|--------------------------|--------------------------------------|
| A0 | Address input (used in X8 mode only) |
| A1-A22 | Address inputs |
| $\overline{\text{BYTE}}$ | Byte/Word Organization Select |
| DQ0-DQ15 | Data Inputs/Outputs |
| E0 | Chip Enable |
| E1 | Chip Enable |
| E2 | Chip Enable |
| $\overline{\text{G}}$ | Output Enable |
| $\overline{\text{RP}}$ | Reset/Power-Down |
| STS | Status/(Ready/Busy) |
| V _{PEN} | Program/Erase Enable |
| $\overline{\text{W}}$ | Write Enable |
| V _{DD} | Supply Voltage |
| V _{DDQ} | Input/Output Supply Voltage |
| V _{SS} | Ground |
| V _{SSQ} | Input/Output Ground |
| NC | Not Connected Internally |
| DU | Do Not Use |

Figure 3. TSOP56 Connections



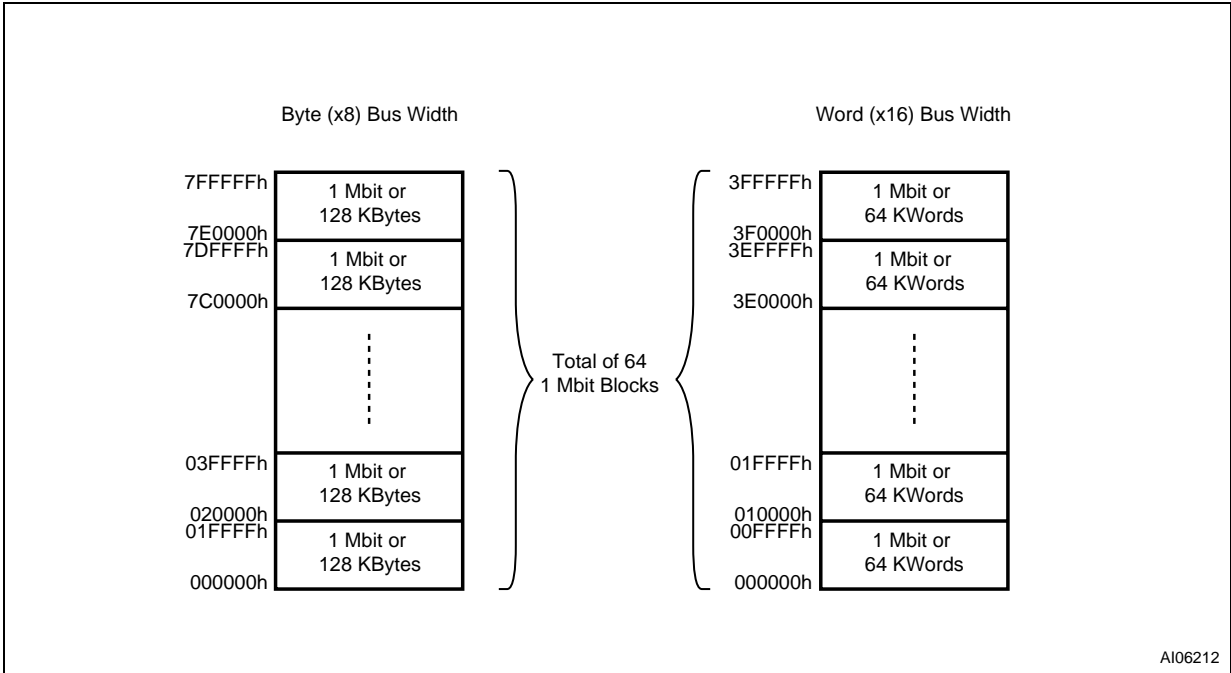
AI05585

Figure 4. TBGA64 Connections (Top view through package)



AI05586b

Figure 5. Block Addresses



Note: Also see [APPENDIX A., Table 23.](#) for a full listing of the Block Addresses

SIGNAL DESCRIPTIONS

See [Figure 2., Logic Diagram](#), and [Table 1., Signal Names](#), for a brief overview of the signals connected to this device.

Address Input (A0). The A0 address input is used to select the higher or lower Byte in X8 mode. It is not used in X16 mode (where A1 is the Lowest Significant bit).

Address Inputs (A1-A22). The A1-A22 Address Inputs are used to select the cells to access in the memory array during Bus Read operations either to read or to program data. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. The device must be enabled (refer to [Table 2., Device Enable](#)) when selecting the addresses. The address inputs are latched on the rising edge of Write Enable or on the first edge of Chip Enables E0, E1 or E2 that disable the device, whichever occurs first.

Data Inputs/Outputs (DQ0-DQ15). The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation, or are used to input the data during a program operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine. When used to input data or Write commands they are latched on the rising edge of Write Enable or the first edge of Chip Enables E0, E1 or E2 that disable the device, whichever occurs first.

When the device is enabled and Output Enable is low, V_{IL} (refer to [Table 2., Device Enable](#)), the data bus outputs data from the memory array, the Electronic Signature, the Block Protection status, the CFI Information or the contents of the Status Register. The data bus is high impedance when the device is deselected, Output Enable is high, V_{IH} , or the Reset/Power-Down signal is low, V_{IL} . When the Program/Erase Controller is active the Ready/Busy status is given on DQ7.

Chip Enables (E0, E1, E2). The Chip Enable inputs E0, E1 and E2 activate the memory control logic, input buffers, decoders and sense amplifiers. The device is selected at the first edge of Chip Enables E0, E1 or E2 that enable the device and deselected at the first edge of Chip Enables E0, E1 or E2 that disable the device. Refer to [Table 2., Device Enable](#) for more details.

When the Chip Enable inputs deselect the memory, power consumption is reduced to the Standby level, I_{DD1} .

Output Enable (\overline{G}). The Output Enable, \overline{G} , gates the outputs through the data output buffers during a read operation. When Output Enable, \overline{G} , is at V_{IH} the outputs are high impedance.

Write Enable (\overline{W}). The Write Enable input, \overline{W} , controls writing to the Command Interface, Input Address and Data latches. Both addresses and data can be latched on the rising edge of Write Enable.

Reset/Power-Down (\overline{RP}). The Reset/Power-Down pin can be used to apply a Hardware Reset to the memory.

A Hardware Reset is achieved by holding Reset/Power-Down Low, V_{IL} , for at least t_{PLPH} . When Reset/Power-Down is Low, V_{IL} , the Status Register information is cleared and the power consumption is reduced to power-down level. The device is deselected and outputs are high impedance. If Reset/Power-Down goes low, V_{IL} , during a Block Erase, a Write to Buffer and Program or a Block Protect/Unprotect the operation is aborted and the data may be corrupted. In this case the STS pin stays low, V_{IL} , for a maximum timing of $t_{PLPH} + t_{PH-BH}$, until the completion of the Reset/Power-Down pulse.

After Reset/Power-Down goes High, V_{IH} , the memory will be ready for Bus Read and Bus Write operations after t_{PHQV} . Note that STS does not fall during a reset, see Ready/Busy Output section.

In an application, it is recommended to associate Reset/Power-Down pin, \overline{RP} , with the reset signal of the microprocessor. Otherwise, if a reset operation occurs while the memory is performing an Erase or Program operation, the memory may output the Status Register information instead of being initialized to the default Asynchronous Random Read.

Byte/Word Organization Select (\overline{BYTE}). The Byte/Word Organization Select pin is used to switch between the x8 and x16 bus widths of the memory. When Byte/Word Organization Select is Low, V_{IL} , the memory is in x8 mode, when it is High, V_{IH} , the memory is in x16 mode.

Status/(Ready/Busy) (STS). The STS signal is an open drain output that can be used to identify the Program/Erase Controller status. It can be configured in two modes:

- Ready/Busy - the pin is Low, V_{OL} , during Program and Erase operations and high impedance when the memory is ready for any Read, Program or Erase operation.
- Status - the pin gives a pulsing signal to indicate the end of a Program or Block Erase operation.

After power-up or reset the STS pin is configured in Ready/Busy mode. The pin can be configured for Status mode using the Configure STS command.

When the Program/Erase Controller is idle, or suspended, STS can float High through a pull-up resistor. The use of an open-drain output allows the STS pins from several memories to be connected to a single pull-up resistor (a Low will indicate that one, or more, of the memories is busy).

STS is not Low during a reset unless the reset was applied when the Program/Erase controller was active

Program/Erase Enable (V_{PEN}). The Program/Erase Enable input, V_{PEN}, is used to protect all blocks, preventing Program and Erase operations from affecting their data.

Program/Erase Enable must be kept High during all Program/Erase Controller operations, otherwise the operations is not guaranteed to succeed and data may become corrupt.

V_{DD} Supply Voltage. V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read, Program and Erase).

V_{DDQ} Supply Voltage. V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

It is recommended to power-up and power-down V_{DD} and V_{DDQ} together to avoid any condition that would result in data corruption.

V_{SS} Ground. Ground, V_{SS}, is the reference for the core power supply. It must be connected to the system ground.

V_{SSQ} Ground. V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ}. V_{SSQ} must be connected to V_{SS}.

Note: Each device in a system should have V_{DD} and V_{DDQ} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 8., AC Measurement Load Circuit.

Table 2. Device Enable

| E2 | E1 | E0 | Device |
|-----------------|-----------------|-----------------|----------|
| V _{IL} | V _{IL} | V _{IL} | Enabled |
| V _{IL} | V _{IL} | V _{IH} | Disabled |
| V _{IL} | V _{IH} | V _{IL} | Disabled |
| V _{IL} | V _{IH} | V _{IH} | Disabled |
| V _{IH} | V _{IL} | V _{IL} | Enabled |
| V _{IH} | V _{IL} | V _{IH} | Enabled |
| V _{IH} | V _{IH} | V _{IL} | Enabled |
| V _{IH} | V _{IH} | V _{IH} | Disabled |

Note: For single device operations, E2 and E1 can be connected to V_{SS}.

BUS OPERATIONS

There are five standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Power-Down and Standby. See [Table 3., Bus Operations](#), for a summary.

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect Bus Write operations.

Bus Read. Bus Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register, the Common Flash Interface and the Block Protection Status.

A valid bus operation involves setting the desired address on the Address inputs, enabling the device (refer to [Table 2., Device Enable](#)), applying a Low signal, V_{IL} , to Output Enable and keeping Write Enable High, V_{IH} . The data read depends on the previous command written to the memory (see Command Interface section).

See Figures 9 and 10 Read AC Waveforms, and Tables 15 and 16 Read AC Characteristics, for details of when the output becomes valid.

Bus Write. Bus Write operations write Commands to the memory or latch addresses and input data to be programmed.

A valid Bus Write operation begins by setting the desired address on the Address Inputs and enabling the device (refer to Chip Enable section).

The Address Inputs are latched by the Command Interface on the rising edge of Write Enable or the

first edge of E0, E1 or E2 that disables the device (refer to [Table 2., Device Enable](#)).

The Data Input/Outputs are latched by the Command Interface on the rising edge of Write Enable or the first edge of E0, E1 or E2 that disable the device whichever occurs first. Output Enable must remain High, V_{IH} , during the Bus Write operation.

See Figures 11 and 12, Write AC Waveforms, and Tables 17 and 18, Write and Chip Enable Controlled Write AC Characteristics, for details of the timing requirements.

Output Disable. The Data Inputs/Outputs are high impedance when the Output Enable is at V_{IH} .

Power-Down. The memory is in Power-Down mode when Reset/Power-Down, \overline{RP} , is Low. The power consumption is reduced to the Power-Down level, I_{DD2} , and the outputs are high impedance, independent of Chip Enable, Output Enable or Write Enable.

Standby. Standby disables most of the internal circuitry, allowing a substantial reduction of the current consumption. The memory is in standby when Chip Enable is at V_{IH} . The power consumption is reduced to the standby level I_{DD1} and the outputs are set to high impedance, independently from the Output Enable or Write Enable inputs.

If Chip Enable switches to V_{IH} during a program or erase operation, the device enters Standby mode when finished.

Table 3. Bus Operations

| Operation | E0, E1 or E2 | \overline{G} | \overline{W} | \overline{RP} | A1-A22 (x16) A0-A22 (x8) | DQ0-DQ15 (x16) DQ0-DQ7 (x8) ⁽¹⁾ |
|----------------|--------------|----------------|----------------|-----------------|-----------------------------|---|
| Bus Read | V_{IL} | V_{IL} | V_{IH} | V_{IH} | Address | Data Output |
| Bus Write | V_{IL} | V_{IH} | V_{IL} | V_{IH} | Address | Data Input |
| Output Disable | V_{IL} | V_{IH} | V_{IH} | V_{IH} | X | High Z |
| Power-Down | X | X | X | V_{IL} | X | High Z |
| Standby | V_{IH} | X | X | V_{IH} | X | High Z |

Note: 1. DQ8-DQ15 are High Z in x8 mode.
2. X = Don't Care V_{IL} or V_{IH} .

READ MODES

Read operations in the M58LW064D are asynchronous. The device outputs the data corresponding to the address latched, that is the memory array, Status Register, Common Flash Interface, Electronic Signature or Block Protection Status depending on the command issued.

During read operations, if the bus is inactive for a time equivalent to t_{AVQV} , the device automatically enters Auto Low Power mode. In this mode the internal supply current is reduced to the Auto Low Power supply current, I_{DD5} . The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Read operations can be performed in two different ways, Random Read (where each Bus Read operation accesses a different Page) and Page Read.

In Page Read mode a Page of data is internally read and stored in a Page Buffer. Each memory page is a 4 Words or 8 Bytes and has the same A3-A22. In x8 mode only A0, A1 and A2 may change, in x16 mode only A1 and A2 may change.

The first read operation within the Page has the normal access time (t_{AVQV}), subsequent reads within the same Page have much shorter access times (t_{AVQV1}). If the Page changes then the normal, longer timings apply again.

See [Figure 10., Page Read AC Waveforms](#), and [Table 16., Page Read AC Characteristics](#), for details on when the outputs become valid.

COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. The Commands are summarized in [Table 4., Commands](#). Refer to [Table 4.](#) in conjunction with the text descriptions below.

After power-up or a Reset operation the memory enters Read mode.

Read Memory Array Command. The Read Memory Array command is used to return the memory to Read mode. One Bus Write cycle is required to issue the Read Memory Array command and return the memory to Read mode. Once the command is issued the memory remains in Read mode until another command is issued. From Read mode Bus Read operations will access the memory array. After power-up or a reset the memory defaults to Read Array mode (Page Read).

While the Program/Erase Controller is executing a Program, Erase, Block Protect, Blocks Unprotect or Protection Register Program operation the memory will not accept the Read Memory Array command until the operation completes.

Read Electronic Signature Command. The Read Electronic Signature command is used to read the Manufacturer Code, the Device Code, the Block Protection Status and the Protection Register. One Bus Write cycle is required to issue the Read Electronic Signature command. Once the command is issued subsequent Bus Read operations read the Manufacturer Code, the Device Code, the Block Protection Status or the Protection Register until another command is issued. Refer to [Table 6., Read Electronic Signature](#), [Tables 7 and 8](#), Word and Byte-wide Read Protection Register and [Figure 6., Protection Register Memory Map](#), for information on the addresses.

Read Query Command. The Read Query Command is used to read data from the Common Flash Interface (CFI) Memory Area. One Bus Write cycle is required to issue the Read Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area. See [APPENDIX B.](#), [Tables 24, 25, 26, 27, 28 and 29](#) for details on the information contained in the Common Flash Interface (CFI) memory area.

Read Status Register Command. The Read Status Register command is used to read the Status Register. One Bus Write cycle is required to issue the Read Status Register command. Once the command is issued subsequent Bus Read operations read the Status Register until another command is issued.

The Status Register information is present on the output data bus (DQ1-DQ7) when the device is enabled and Output Enable is Low, V_{IL} .

See the section on the Status Register and [Table 10.](#) for details on the definitions of the Status Register bits

Clear Status Register Command. The Clear Status Register command can be used to reset bits SR1, SR3, SR4 and SR5 in the Status Register to '0'. One Bus Write is required to issue the Clear Status Register command.

The bits in the Status Register are sticky and do not automatically return to '0' when a new Write to Buffer and Program, Erase, Block Protect, Block Unprotect or Protection Register Program command is issued. If any error occurs then it is essential to clear any error bits in the Status Register by issuing the Clear Status Register command before attempting a new Program, Erase or Resume command.

Block Erase Command. The Block Erase command can be used to erase a block. It sets all of the bits in the block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two Bus Write operations are required to issue the command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Erase operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored. Typical Erase times are given in [Table 9.](#)

See [APPENDIX C.](#), [Figure 18., Erase Flowchart and Pseudo Code](#), for a suggested flowchart on using the Block Erase command.

Word/Byte Program Command. The Word/Byte Program command is used to program a single Word or Byte in the memory array. Two Bus Write operations are required to issue the command; the first write cycle sets up the Word Program command, the second write cycle latches the address and data to be programmed in the internal state machine and starts the Program/Erase Controller.

If the block being programmed is protected an error will be set in the Status Register and the operation will abort without affecting the data in the

memory array. The block must be unprotected using the Blocks Unprotect command or by using the Blocks Temporary Unprotect feature of the Reset/Power-Down pin, RP.

Write to Buffer and Program Command. The Write to Buffer and Program command is used to program the memory array.

Up to 16 Words/32 Bytes can be loaded into the Write Buffer and programmed into the memory. Each Write Buffer has the same A5-A22 addresses. In Byte-wide mode only A0-A4 may change in Word-wide mode only A1-A4 may change.

Four successive steps are required to issue the command.

1. One Bus Write operation is required to set up the Write to Buffer and Program Command. Issue the set up command with the selected memory Block Address where the program operation should occur (any address in the block where the values will be programmed can be used). Any Bus Read operations will start to output the Status Register after the 1st cycle.
2. Use one Bus Write operation to write the same block address along with the value N on the Data Inputs/Output, where N+1 is the number of Words/Bytes to be programmed.
3. Use N+1 Bus Write operations to load the address and data for each Word into the Write Buffer. See the constraints on the address combinations listed below. The addresses must have the same A5-A22.
4. Finally, use one Bus Write operation to issue the final cycle to confirm the command and start the Program operation.

Invalid address combinations or failing to follow the correct sequence of Bus Write cycles will set an error in the Status Register and abort the operation without affecting the data in the memory array. The Status Register should be cleared before re-issuing the command.

If the block being programmed is protected an error will be set in the Status Register and the operation will abort without affecting the data in the memory array. The block must be unprotected using the Blocks Unprotect command.

See [APPENDIX C., Figure 16., Write to Buffer and Program Flowchart and Pseudo Code](#), for a suggested flowchart on using the Write to Buffer and Program command.

Program/Erase Suspend Command. The Program/Erase Suspend command is used to pause a Word/Byte Program, Write to Buffer and Program or Erase operation. The command will only be accepted during a Program or an Erase operation. It can be issued at any time during an Erase opera-

tion but will only be accepted during a Word Program or Write to Buffer and Program command if the Program/Erase Controller is running.

One Bus Write cycle is required to issue the Program/Erase Suspend command and pause the Program/Erase Controller. Once the command is issued it is necessary to poll the Program/Erase Controller Status bit (SR7) to find out when the Program/Erase Controller has paused; no other commands will be accepted until the Program/Erase Controller has paused. After the Program/Erase Controller has paused, the memory will continue to output the Status Register until another command is issued.

During the polling period between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing it is possible for the operation to complete. Once the Program/Erase Controller Status bit (SR7) indicates that the Program/Erase Controller is no longer active, the Program Suspend Status bit (SR2) or the Erase Suspend Status bit (SR6) can be used to determine if the operation has completed or is suspended. For timing on the delay between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing see [Table 9](#).

During Program/Erase Suspend the Read Memory Array, Read Status Register, Read Electronic Signature, Read Query and Program/Erase Resume commands will be accepted by the Command Interface. Additionally, if the suspended operation was Erase then the Write to Buffer and Program, and the Program Suspend commands will also be accepted. When a program operation is completed inside a Block Erase Suspend the Read Memory Array command must be issued to reset the device in Read mode, then the Erase Resume command can be issued to complete the whole sequence. Only the blocks not being erased may be read or programmed correctly.

See [APPENDIX C., Figure 17., Program Suspend & Resume Flowchart and Pseudo Code](#), and [Figure 19., Erase Suspend & Resume Flowchart and Pseudo Code](#), for suggested flowcharts on using the Program/Erase Suspend command.

Program/Erase Resume Command. The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend operation has paused it. One Bus Write cycle is required to issue the Program/Erase Resume command. Once the command is issued subsequent Bus Read operations read the Status Register.

Block Protect Command. The Block Protect command is used to protect a block and prevent Program or Erase operations from changing the data in it. Two Bus Write cycles are required to issue the Block Protect command; the second Bus

Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Block Protect operation the memory will only accept the Read Status Register command. All other commands will be ignored. Typical Block Protection times are given in [Table 9](#).

The Block Protection bits are non-volatile, once set they remain set through reset and power-down/power-up. They are cleared by a Blocks Unprotect command.

See [APPENDIX C., Figure 20., Block Protect Flowchart and Pseudo Code](#), for a suggested flowchart on using the Block Protect command.

Blocks Unprotect Command. The Blocks Unprotect command is used to unprotect all of the blocks. Two Bus Write cycles are required to issue the Blocks Unprotect command; the second Bus Write cycle starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Block Unprotect operation the memory will only accept the Read Status Register command. All other commands will be ignored. Typical Block Protection times are given in [Table 9](#).

See [APPENDIX C., Figure 21., Blocks Unprotect Flowchart and Pseudo Code](#), for a suggested flowchart on using the Block Unprotect command.

Protection Register Program Command. The Protection Register Program command is used to Program the 64 bit user segment of the Protection Register. Two write cycles are required to issue the Protection Register Program command.

- The first bus cycle sets up the Protection Register Program command.
- The second latches the Address and the Data to be written to the Protection Register and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started.

The user-programmable segment can be locked by programming bit 1 of the Protection Register Lock location to '0' (see [Table 7](#) and [Table 8](#) for Word-wide and Byte-wide protection addressing). Bit 0 of the Protection Register Lock location locks the factory programmed segment and is programmed to '0' in the factory. The locking of the Protection Register is not reversible, once the lock bits are programmed no further changes can be made to the values stored in the Protection Register, see [Figure 6., Protection Register Memory Map](#). Attempting to program a previously protected Protection Register will result in a Status Register error.

The Protection Register Program cannot be suspended. See [APPENDIX C., Figure 22., Protection Register Program Flowchart and Pseudo Code](#), for the flowchart for using the Protection Register Program command.

Configure STS Command.

The Configure STS command is used to configure the Status/(Ready/Busy) pin. After power-up or reset the STS pin is configured in Ready/Busy mode. The pin can be configured in Status mode using the Configure STS command (refer to Status/(Ready/Busy) section for more details.

Two write cycles are required to issue the Configure STS command.

- The first bus cycle sets up the Configure STS command.
- The second specifies one of the four possible configurations (refer to [Table 5., Configuration Codes](#)):
 - Ready/Busy mode
 - Pulse on Erase complete mode
 - Pulse on Program complete mode
 - Pulse on Erase or Program complete mode

The device will not accept the Configure STS command while the Program/Erase controller is busy or during Program/Erase Suspend. When STS pin is pulsing it remains Low for a typical time of 250ns. Any invalid Configuration Code will set an error in the Status Register.

Table 4. Commands

| Command | Cycles | Bus Operations | | | | | | | | | | | |
|-----------------------------|--------|----------------|-------|------------|-----------|--------------------|--------------------|------------|-------|------|-------|-------|------|
| | | 1st Cycle | | | 2nd Cycle | | | Subsequent | | | Final | | |
| | | Op. | Addr. | Data | Op. | Addr. | Data | Op. | Addr. | Data | Op. | Addr. | Data |
| Read Memory Array | ≥ 2 | Write | X | FFh | Read | RA | RD | | | | | | |
| Read Electronic Signature | ≥ 2 | Write | X | 90h | Read | IDA ⁽²⁾ | IDD ⁽²⁾ | | | | | | |
| Read Status Register | 2 | Write | X | 70h | Read | X | SRD | | | | | | |
| Read Query | ≥ 2 | Write | X | 98h | Read | QA ⁽³⁾ | QD ⁽³⁾ | | | | | | |
| Clear Status Register | 1 | Write | X | 50h | | | | | | | | | |
| Block Erase | 2 | Write | X | 20h | Write | BA | D0 | | | | | | |
| Word/Byte Program | 2 | Write | X | 40h 10h | Write | PA | PD | | | | | | |
| Write to Buffer and Program | 4 + N | Write | BA | E8h | Write | BA | N | Write | PA | PD | Write | X | D0h |
| Program/Erase Suspend | 1 | Write | X | B0h | | | | | | | | | |
| Program/Erase Resume | 1 | Write | X | D0h | | | | | | | | | |
| Block Protect | 2 | Write | X | 60h | Write | BA | 01h | | | | | | |
| Blocks Unprotect | 2 | Write | X | 60h | Write | X | D0h | | | | | | |
| Protection Register Program | 2 | Write | X | C0h | Write | PRA | PRD | | | | | | |
| Configure STS command | 2 | Write | X | B8h | Write | X | CC | | | | | | |

Note: 1. X Don't Care; RA Read Address, RD Read Data, IDA Identifier Address, IDD Identifier Data, SRD Status Register Data, PA Program Address; PD Program Data, QA Query Address, QD Query Data, BA Any address in the Block, PRA Protection register address, PRD Protection Register Data, CC Configuration Code.

2. For Identifier addresses and data refer to [Table 6., Read Electronic Signature](#).

3. For Query Address and Data refer to [APPENDIX B., COMMON FLASH INTERFACE - CFI](#).

Table 5. Configuration Codes

| Configuration Code | DQ1 | DQ2 | Mode | STS Pin | Description |
|--------------------|-----|-----|------------------------------------|--|--|
| 00h | 0 | 0 | Ready/Busy | V _{OL} during P/E operations Hi-Z when the memory is ready | The STS pin is Low during Program and Erase operations and high impedance when the memory is ready for any Read, Program or Erase operation. |
| 01h | 0 | 1 | Pulse on Erase complete | Pulse Low then High when operation completed ⁽²⁾ | Supplies a system interrupt pulse at the end of a Block Erase operation. |
| 02h | 1 | 0 | Pulse on Program complete | | Supplies a system interrupt pulse at the end of a Program operation. |
| 03h | 1 | 1 | Pulse on Erase or Program complete | | Supplies a system interrupt pulse at the end of a Block Erase or Program operation. |

Note: 1. DQ2-DQ7 are reserved

2. When STS pin is pulsing it remains Low for a typical time of 250ns.

Table 6. Read Electronic Signature

| Code | Bus Width | Address (A22-A1) ⁽³⁾ | Data (DQ15-DQ0) |
|-------------------------|-----------|---------------------------------|--|
| Manufacturer Code | x8 | 000000h | 20h |
| | x16 | | 0020h |
| Device Code | x8 | 000001h | 17h |
| | x16 | | 0017h |
| Block Protection Status | x8 | SBA ⁽¹⁾ +02h | 00h (Block Unprotected) 01h (Block Protected) |
| | x16 | | 0000h (Block Unprotected) 0001h (Block Protected) |
| Protection Register | x8, x16 | 000080h ⁽²⁾ | PRD ⁽¹⁾ |

Note: 1. SBA is the Start Base Address of each block, PRD is Protection Register Data.
 2. Base Address, refer to Figure 6. and Tables 7 and 8 for more information.
 3. A0 is not used in Read Electronic Signature in either x8 or x16 mode. The data is always presented on the lower byte in x16 mode.

Figure 6. Protection Register Memory Map

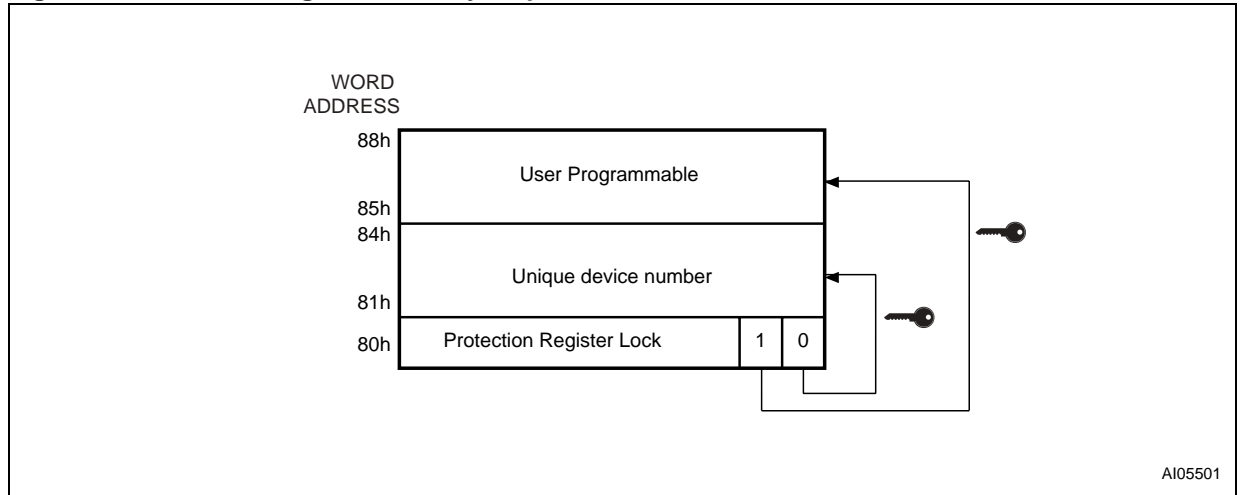


Table 7. Word-Wide Read Protection Register

| Word | Use | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
|------|---------------------|----|----|----|----|----|----|----|----|
| Lock | Factory, User | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | Factory (Unique ID) | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | Factory (Unique ID) | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 2 | Factory (Unique ID) | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 3 | Factory (Unique ID) | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 4 | User | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 5 | User | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 6 | User | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 7 | User | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

Table 8. Byte-Wide Read Protection Register

| Word | Use | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
|------|---------------------|----|----|----|----|----|----|----|----|
| Lock | Factory, User | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Lock | Factory, User | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | Factory (Unique ID) | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | Factory (Unique ID) | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | Factory (Unique ID) | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 3 | Factory (Unique ID) | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 4 | Factory (Unique ID) | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 5 | Factory (Unique ID) | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 6 | Factory (Unique ID) | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 7 | Factory (Unique ID) | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 8 | User | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 9 | User | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| A | User | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| B | User | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| C | User | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| D | User | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| E | User | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| F | User | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

Table 9. Program, Erase Times and Program Erase Endurance Cycles

| Parameters | M58LW064D | | | Unit |
|---|-----------|----------------------|--------------------|--------|
| | Min | Typ ^(1,2) | Max ⁽²⁾ | |
| Block (1Mb) Erase | | 1.2 | 4.8 ⁽⁴⁾ | s |
| Chip Program (Write to Buffer) | | 49 | 145 ⁽⁴⁾ | s |
| Chip Erase Time | | 74 | 220 ⁽⁴⁾ | s |
| Program Write Buffer | | 192 ⁽³⁾ | 576 ⁽⁴⁾ | μs |
| Word/Byte Program Time (Word/Byte Program command) | | 16 | 48 ⁽⁴⁾ | μs |
| Program Suspend Latency Time | | 1 | 20 ⁽⁵⁾ | μs |
| Erase Suspend Latency Time | | 1 | 25 ⁽⁵⁾ | μs |
| Block Protect Time | | 18 | 30 ⁽⁵⁾ | μs |
| Blocks Unprotect Time | | 0.75 | 1.2 ⁽⁵⁾ | s |
| Program/Erase Cycles (per block) | 100,000 | | | cycles |
| Data Retention | 20 | | | years |

Note: 1. Typical values measured at room temperature and nominal voltages.

2. Sampled, but not 100% tested.

3. Effective byte programming time 6μs, effective word programming time 12μs.

4. Maximum value measured at worst case conditions for both temperature and V_{DD} after 100,000 program/erase cycles.

5. Maximum value measured at worst case conditions for both temperature and V_{DD}.

STATUS REGISTER

The Status Register provides information on the current or previous Program, Erase, Block Protect or Blocks Unprotect operation. The various bits in the Status Register convey information and errors on the operation. They are output on DQ7-DQ0.

To read the Status Register the Read Status Register command can be issued. The Status Register is automatically read after Program, Erase, Block Protect, Blocks Unprotect and Program/Erase Resume commands. The Status Register can be read from any address.

The contents of the Status Register can be updated during an Erase or Program operation by toggling the Output Enable pin or by de-activating and then reactivating the device (refer to [Table 2., Device Enable](#)).

Status Register bits SR5, SR4, SR3 and SR1 are associated with various error conditions and can only be reset with the Clear Status Register command. The Status Register bits are summarized in [Table 10., Status Register Bits](#). Refer to [Table 10.](#) in conjunction with the following text descriptions.

Program/Erase Controller Status Bit (SR7). The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive. When the Program/Erase Controller Status bit is Low, V_{OL} , the Program/Erase Controller is active and all other Status Register bits are High Impedance; when the bit is High, V_{OH} , the Program/Erase Controller is inactive.

The Program/Erase Controller Status is Low immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is High.

During Program, Erase, Block Protect and Blocks Unprotect operations the Program/Erase Controller Status bit can be polled to find the end of the operation. The other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is High.

After the Program/Erase Controller completes its operation the Erase Status, Program Status and Block Protection Status bits should be tested for errors.

Erase Suspend Status Bit (SR6). The Erase Suspend Status bit indicates that an Erase operation has been suspended and is waiting to be resumed. The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Erase Suspend Status bit is Low, V_{OL} , the Program/Erase Controller is active or has completed its operation; when the bit is High, V_{OH} , a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns Low.

Erase Status Bit (SR5). The Erase Status bit can be used to identify if the memory has failed to verify that the block has erased correctly or that all blocks have been unprotected successfully. The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

When the Erase Status bit is Low, V_{OL} , the memory has successfully verified that the block has erased correctly or all blocks have been unprotected successfully. When the Erase Status bit is High, V_{OH} , the erase operation has failed. Depending on the cause of the failure other Status Register bits may also be set to High, V_{OH} .

- If only the Erase Status bit (SR5) is set High, V_{OH} , then the Program/Erase Controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly or that all the blocks have been unprotected successfully.
- If the failure is due to an erase or blocks unprotect with V_{PEN} low, V_{OL} , then V_{PEN} Status bit (SR3) is also set High, V_{OH} .
- If the failure is due to an erase on a protected block then Block Protection Status bit (SR1) is also set High, V_{OH} .
- If the failure is due to a program or erase incorrect command sequence then Program Status bit (SR4) is also set High, V_{OH} .

Once set High, the Erase Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Status Bit (SR4). The Program Status bit is used to identify a Program or Block Protect failure. The Program Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

When the Program Status bit is Low, V_{OL} , the memory has successfully verified that the Write Buffer has programmed correctly or the block is protected. When the Program Status bit is High, V_{OH} , the program or block protect operation has failed. Depending on the cause of the failure other Status Register bits may also be set to High, V_{OH} .

- If only the Program Status bit (SR4) is set High, V_{OH} , then the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that the Write Buffer has programmed correctly or that the Block is protected.
- If the failure is due to a program or block protect with V_{PEN} low, V_{OL} , then V_{PEN} Status bit (SR3) is also set High, V_{OH} .
- If the failure is due to a program on a protected block then Block Protection Status bit (SR1) is also set High, V_{OH} .
- If the failure is due to a program or erase incorrect command sequence then Erase Status bit (SR5) is also set High, V_{OH} .

Once set High, the Program Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

V_{PEN} Status Bit (SR3). The V_{PEN} Status bit can be used to identify if a Program, Erase, Block Protection or Block Unprotection operation has been attempted when V_{PEN} is Low, V_{IL} .

When the V_{PEN} Status bit is Low, V_{OL} , no Program, Erase, Block Protection or Block Unprotection operations have been attempted with V_{PEN} Low, V_{IL} , since the last Clear Status Register command, or hardware reset. When the V_{PEN} Status bit is High, V_{OH} , a Program, Erase, Block Protection or Block Unprotection operation has been attempted with V_{PEN} Low, V_{IL} .

Once set High, the V_{PEN} Status bit can only be reset by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program, Erase, Block Protection or Block Unprotection command is issued, otherwise the new command will appear to fail.

Program Suspend Status Bit (SR2). The Program Suspend Status bit indicates that a Program operation has been suspended and is waiting to be resumed. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Program Suspend Status bit is Low, V_{OL} , the Program/Erase Controller is active or has completed its operation; when the bit is High, V_{OH} , a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns Low.

Block Protection Status Bit (SR1). The Block Protection Status bit can be used to identify if a Program or Erase operation has tried to modify the contents of a protected block.

When the Block Protection Status bit is Low, V_{OL} , no Program or Erase operations have been attempted to protected blocks since the last Clear Status Register command or hardware reset; when the Block Protection Status bit is High, V_{OH} , a Program (Program Status bit SR4 set High) or Erase (Erase Status bit SR5 set High) operation has been attempted on a protected block.

Once set High, the Block Protection Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Reserved (SR0). Bit SR0 of the Status Register is reserved. Its value should be masked.

Table 10. Status Register Bits

| OPERATION | SR 7 | SR 6 | SR 5 | SR 4 | SR 3 | SR 2 | SR 1 | Result (Hex) |
|--|------|------|------|------|------|------|------|--------------|
| Program/Erase Controller active | 0 | Hi-Z | | | | | | N/A |
| Write Buffer not ready | 0 | Hi-Z | | | | | | N/A |
| Write Buffer ready | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 80h |
| Write Buffer ready in Erase Suspend | 1 | 1 | 0 | 0 | 0 | 0 | 0 | C0h |
| Program suspended | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 84h |
| Program suspended in Erase Suspend | 1 | 1 | 0 | 0 | 0 | 1 | 0 | C4h |
| Program/Block Protect completed successfully | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 80h |
| Program completed successfully in Erase Suspend | 1 | 1 | 0 | 0 | 0 | 0 | 0 | C0h |
| Program/Block protect failure due to incorrect command sequence | 1 | 0 | 1 | 1 | 0 | 0 | 0 | B0h |
| Program failure due to incorrect command sequence in Erase Suspend | 1 | 1 | 1 | 1 | 0 | 0 | 0 | F0h |
| Program/Block Protect failure due to V _{PEN} error | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 98h |
| Program failure due to V _{PEN} error in Erase Suspend | 1 | 1 | 0 | 1 | 1 | 0 | 0 | D8h |
| Program failure due to Block Protection | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 92h |
| Program failure due to Block Protection in Erase Suspend | 1 | 1 | 0 | 1 | 0 | 0 | 1 | D2h |
| Program/Block Protect failure due to cell failure | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 90h |
| Program failure due to cell failure in Erase Suspend | 1 | 1 | 0 | 1 | 0 | 0 | 0 | D0h |
| Erase Suspended | 1 | 1 | 0 | 0 | 0 | 0 | 0 | C0h |
| Erase/Blocks Unprotect completed successfully | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 80h |
| Erase/Blocks Unprotect failure due to incorrect command sequence | 1 | 0 | 1 | 1 | 0 | 0 | 0 | B0h |
| Erase/Blocks Unprotect failure due to V _{PEN} error | 1 | 0 | 1 | 0 | 1 | 0 | 0 | A8h |
| Erase failure due to Block Protection | 1 | 0 | 1 | 0 | 0 | 0 | 1 | A2h |
| Erase/Blocks Unprotect failure due to failed cells in Block | 1 | 0 | 1 | 0 | 0 | 0 | 0 | A0h |
| Configure STS error due to invalid configuration code | 1 | 0 | 1 | 1 | 0 | 0 | 0 | B0h |

MAXIMUM RATING

Stressing the device above the ratings listed in [Table 11.](#), [Absolute Maximum Ratings](#), may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is

not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 11. Absolute Maximum Ratings

| Symbol | Parameter | Value | | Unit |
|------------------------------------|-----------------------------------|-------|-----------------------|------|
| | | Min | Max | |
| T _{BIAS} | Temperature Under Bias | -40 | 125 | °C |
| T _{STG} | Storage Temperature | -55 | 150 | °C |
| T _{LEAD} | Lead Temperature during Soldering | | (1) | °C |
| V _{IO} | Input or Output Voltage | -0.6 | V _{DDQ} +0.6 | V |
| V _{DD} , V _{DDQ} | Supply Voltage | -0.6 | 5.0 | V |
| I _{OSC} | Output Short-circuit Current | | 100 ⁽²⁾ | mA |

Note: 1. Compliant with the JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. Maximum one output short-circuited at a time and for no longer than 1 second.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measure-

ment Conditions summarized in [Table 12., Operating and AC Measurement Conditions](#). Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 12. Operating and AC Measurement Conditions

| Parameter | M58LW064D | | Units | |
|---|----------------|-----|-------|----|
| | Min | Max | | |
| Supply Voltage (V_{DD}) | 2.7 | 3.6 | V | |
| Input/Output Supply Voltage (V_{DDQ}) | 2.7 | 3.6 | V | |
| Ambient Temperature (T_A) | Grade 1 | 0 | 70 | °C |
| | Grade 6 | -40 | 85 | °C |
| Load Capacitance (C_L) | 30 | | pF | |
| Input Pulses Voltages | 0 to V_{DDQ} | | V | |
| Input and Output Timing Ref. Voltages | 0.5 V_{DDQ} | | V | |

Figure 7. AC Measurement Input Output Waveform

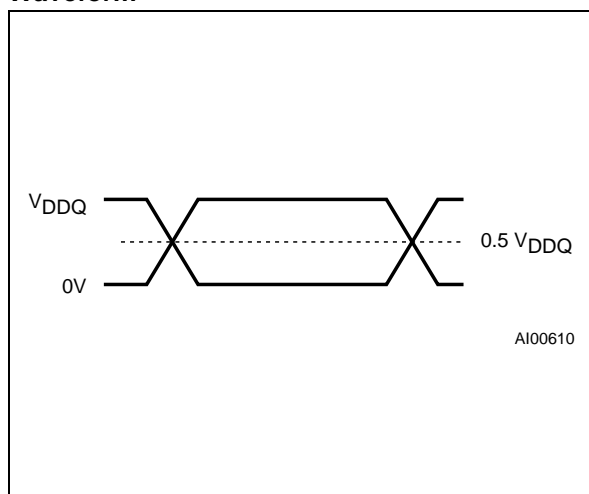


Figure 8. AC Measurement Load Circuit

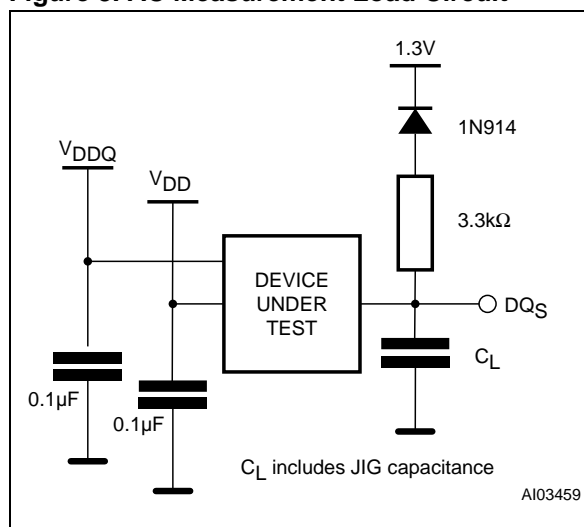


Table 13. Capacitance

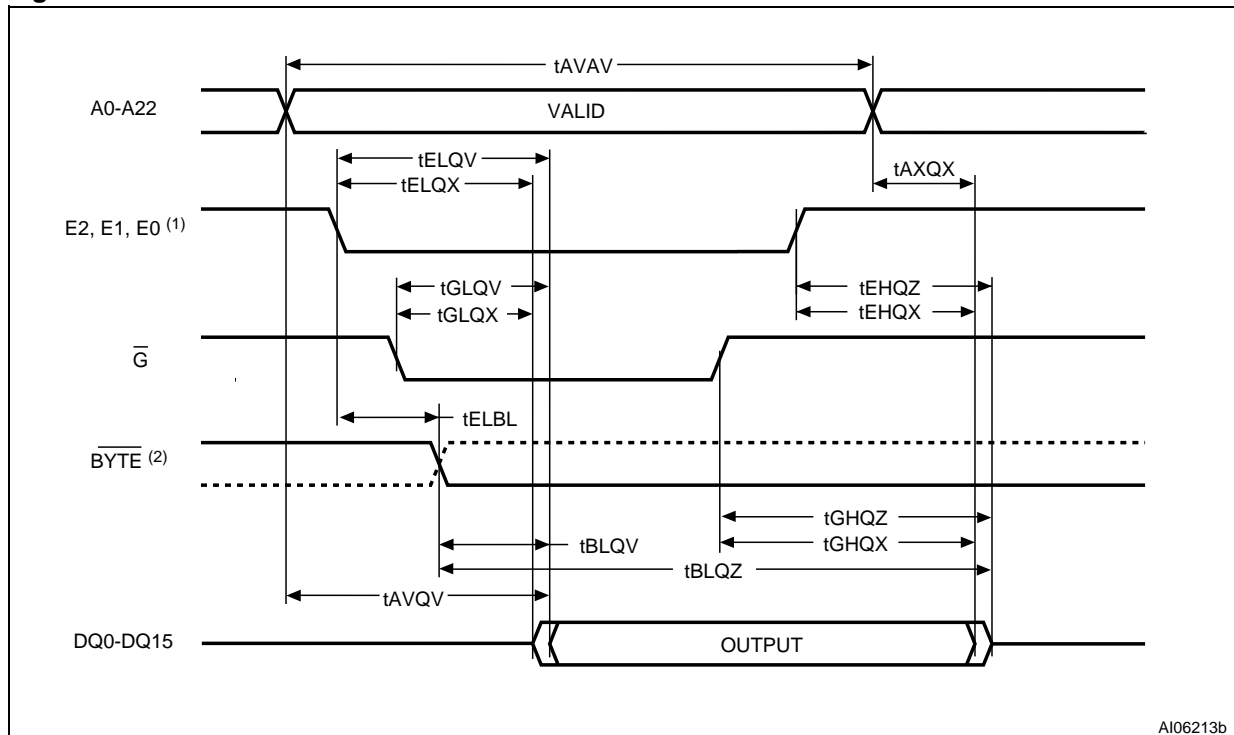
| Symbol | Parameter | Test Condition | Typ | Max | Unit |
|-----------|--------------------|----------------|-----|-----|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ | 6 | 8 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0V$ | 8 | 12 | pF |

Note: 1. $T_A = 25^\circ C$, $f = 1$ MHz
 2. Sampled only, not 100% tested.

Table 14. DC Characteristics

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|------------|---|--|-----------------|-----------------|---------|
| I_{LI} | Input Leakage Current | $0V \leq V_{IN} \leq V_{DDQ}$ | | ± 1 | μA |
| I_{LO} | Output Leakage Current | $0V \leq V_{OUT} \leq V_{DDQ}$ | | ± 5 | μA |
| I_{DD} | Supply Current (Random Read) | $\bar{E} = V_{IL}, f=5MHz$ | | 20 | mA |
| I_{DDO} | Supply Current (Page Read) | $\bar{E} = V_{IL}, f=33MHz$ | | 29 | mA |
| I_{DD1} | Supply Current (Standby) | $\bar{E} = V_{IH}, \overline{RP} = V_{IH}$ | | 40 | μA |
| I_{DD5} | Supply Current (Auto Low-Power) | $\bar{E} = V_{IL}, \overline{RP} = V_{IH}$ | | 40 | μA |
| I_{DD2} | Supply Current (Reset/Power-Down) | $\overline{RP} = V_{IL}$ | | 40 | μA |
| I_{DD3} | Supply Current (Program or Erase, Block Protect, Block Unprotect) | Program or Erase operation in progress | | 30 | mA |
| I_{DD4} | Supply Current (Erase/Program Suspend) | $\bar{E} = V_{IH}$ | | 40 | μA |
| V_{IL} | Input Low Voltage | | -0.5 | 0.8 | V |
| V_{IH} | Input High Voltage | | 2 | $V_{DDQ} + 0.5$ | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 100\mu A$ | | 0.2 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -100\mu A$ | $V_{DDQ} - 0.2$ | | V |
| V_{LKO} | V_{DD} Supply Voltage (Erase and Program lockout) | | 2 | | V |
| V_{PENH} | V_{PEN} Supply Voltage (block erase, program and block protect) | | 2.7 | 3.6 | V |

Figure 9. Random Read AC Waveforms

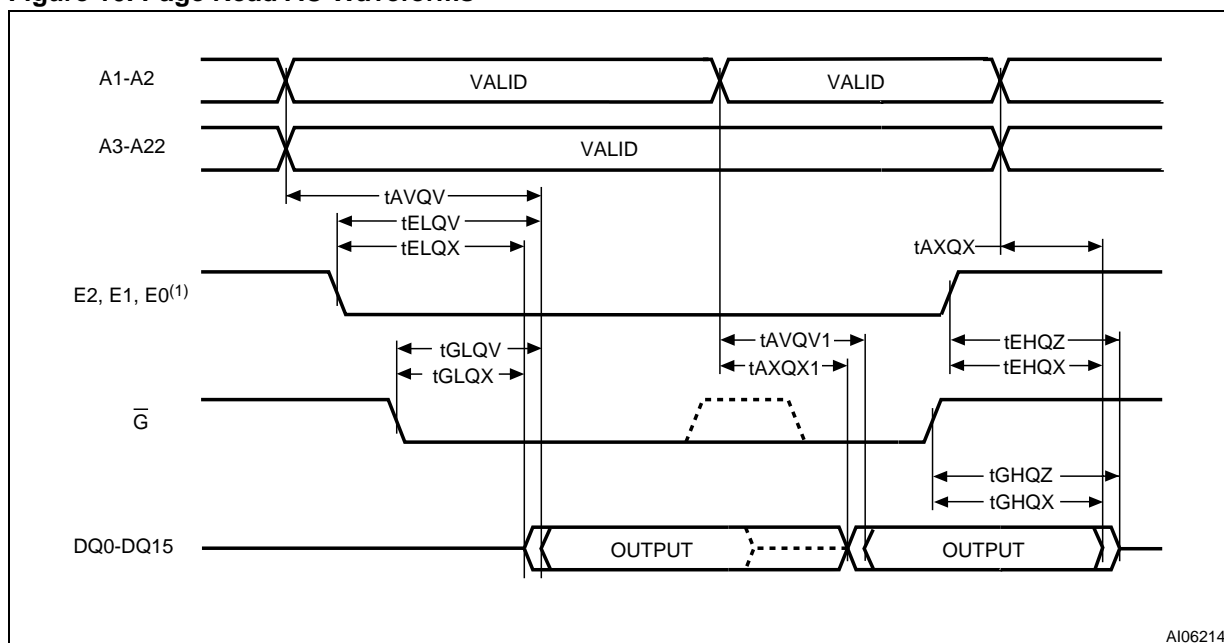


Note: 1. V_{IH} = Device Disabled (first edge of E0, E1 or E2), V_{IL} = Device Enabled (first edge of E0, E1 or E2). Refer to Table 2. for more details.
 2. BYTE can be Low or High.

Table 15. Random Read AC Characteristics.

| Symbol | Parameter | | M58LW064D | |
|--------|---|-----|-----------|------|
| | | | 110 | Unit |
| tAVAV | Address Valid to Address Valid | Min | 110 | ns |
| tAVQV | Address Valid to Output Valid | Max | 110 | ns |
| tAXQX | Address Transition to Output Transition | Min | 0 | ns |
| tBLQV | Byte Low (or High) to Output Valid | Max | 1 | µs |
| tBLQZ | Byte Low (or High) to Output Hi-Z | Max | 1 | µs |
| tEHQX | Chip Enable High to Output Transition | Min | 0 | ns |
| tEHQZ | Chip Enable High to Output Hi-Z | Max | 25 | ns |
| tELBL | Chip Enable Low to Byte Low (or High) | Max | 10 | ns |
| tELQX | Chip Enable Low to Output Transition | Min | 0 | ns |
| tELQV | Chip Enable Low to Output Valid | Max | 110 | ns |
| tGHQX | Output Enable High to Output Transition | Min | 0 | ns |
| tGHQZ | Output Enable High to Output Hi-Z | Max | 15 | ns |
| tGLQX | Output Enable Low to Output Transition | Min | 0 | ns |
| tGLQV | Output Enable Low to Output Valid | Max | 25 | ns |

Figure 10. Page Read AC Waveforms



AI06214

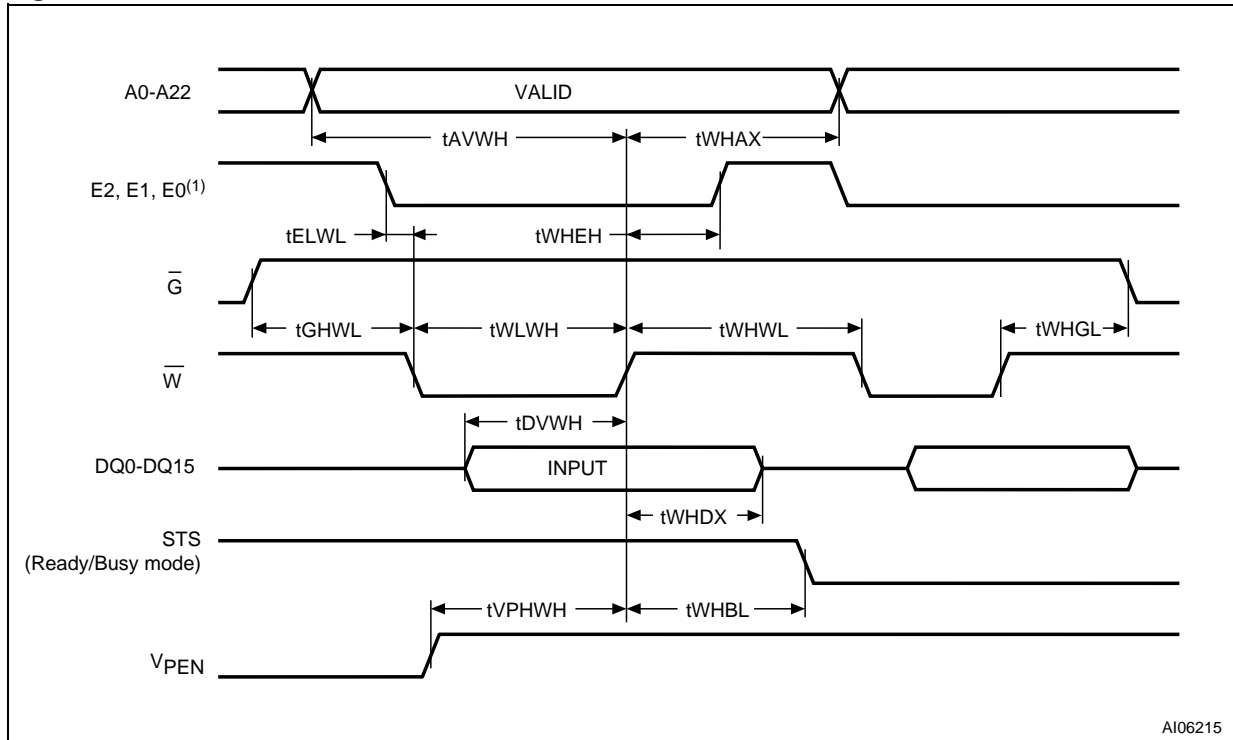
Note: 1. V_{IH} = Device Disabled (first edge of E0, E1 or E2), V_{IL} = Device Enabled (first edge of E0, E1 or E2). Refer to Table 2. for more details.

Table 16. Page Read AC Characteristics

| Symbol | Parameter | | M58LW064D | |
|-------------|---|-----|-----------|------|
| | | | 110 | Unit |
| t_{AXQX1} | Address Transition to Output Transition | Min | 6 | ns |
| t_{AVQV1} | Address Valid to Output Valid | Max | 25 | ns |

Note: For other timings see Table 15., Random Read AC Characteristics.

Figure 11. Write AC Waveform, Write Enable Controlled

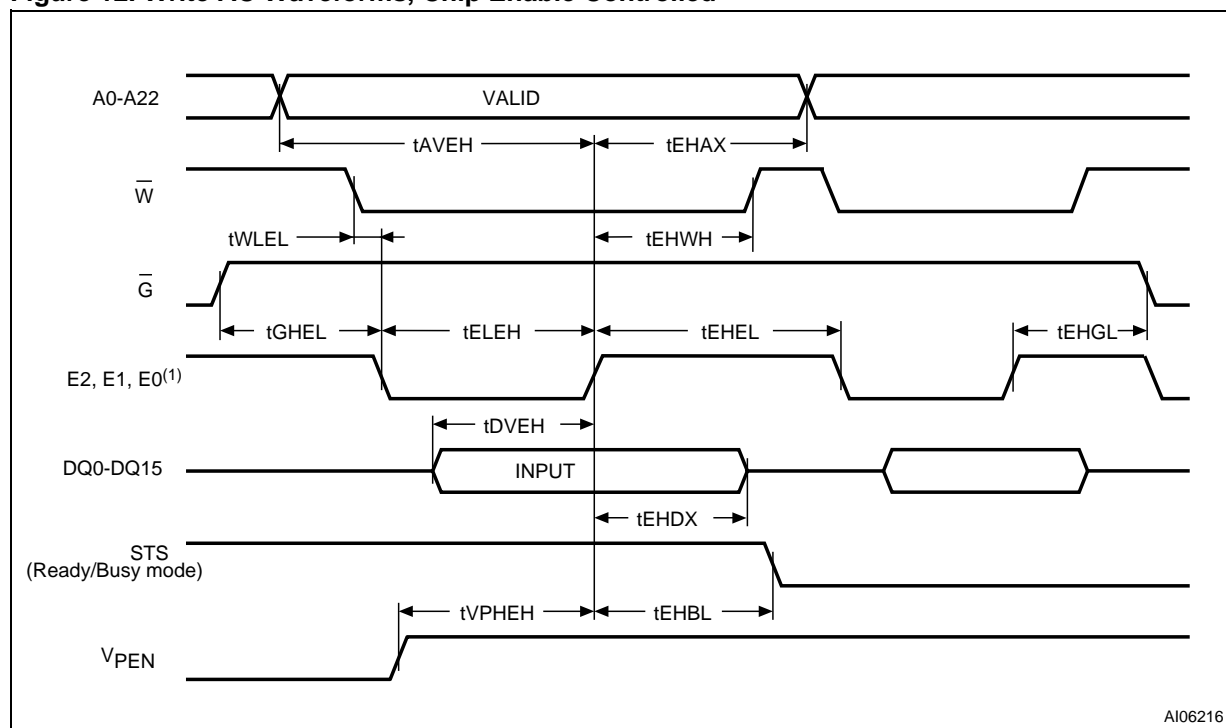


Note: 1. V_{IH} = Device Disabled (first edge of E0, E1 or E2), V_{IL} = Device Enabled (first edge of E0, E1 or E2). Refer to Table 2. for more details.

Table 17. Write AC Characteristics, Write Enable Controlled

| Symbol | Parameter | | M58LW064D | |
|-------------|--|-----|-----------|------|
| | | | 110 | Unit |
| t_{AVWH} | Address Valid to Write Enable High | Min | 50 | ns |
| $t_{D VWH}$ | Data Input Valid to Write Enable High | Min | 50 | ns |
| t_{ELWL} | Chip Enable Low to Write Enable Low | Min | 0 | ns |
| t_{VPHWH} | Program/Erase Enable High to Write Enable High | Min | 0 | ns |
| t_{WHAX} | Write Enable High to Address Transition | Min | 0 | ns |
| t_{WHBL} | Write Enable High to Status/(Ready/Busy) low | Max | 500 | ns |
| t_{WHDX} | Write Enable High to Input Transition | Min | 0 | ns |
| t_{WHEH} | Write Enable High to Chip Enable High | Min | 0 | ns |
| t_{GHWL} | Output Enable High to Write Enable Low | Min | 20 | ns |
| t_{WHGL} | Write Enable High to Output Enable Low | Min | 35 | ns |
| t_{WHWL} | Write Enable High to Write Enable Low | Min | 30 | ns |
| t_{WLWH} | Write Enable Low to Write Enable High | Min | 70 | ns |

Figure 12. Write AC Waveforms, Chip Enable Controlled



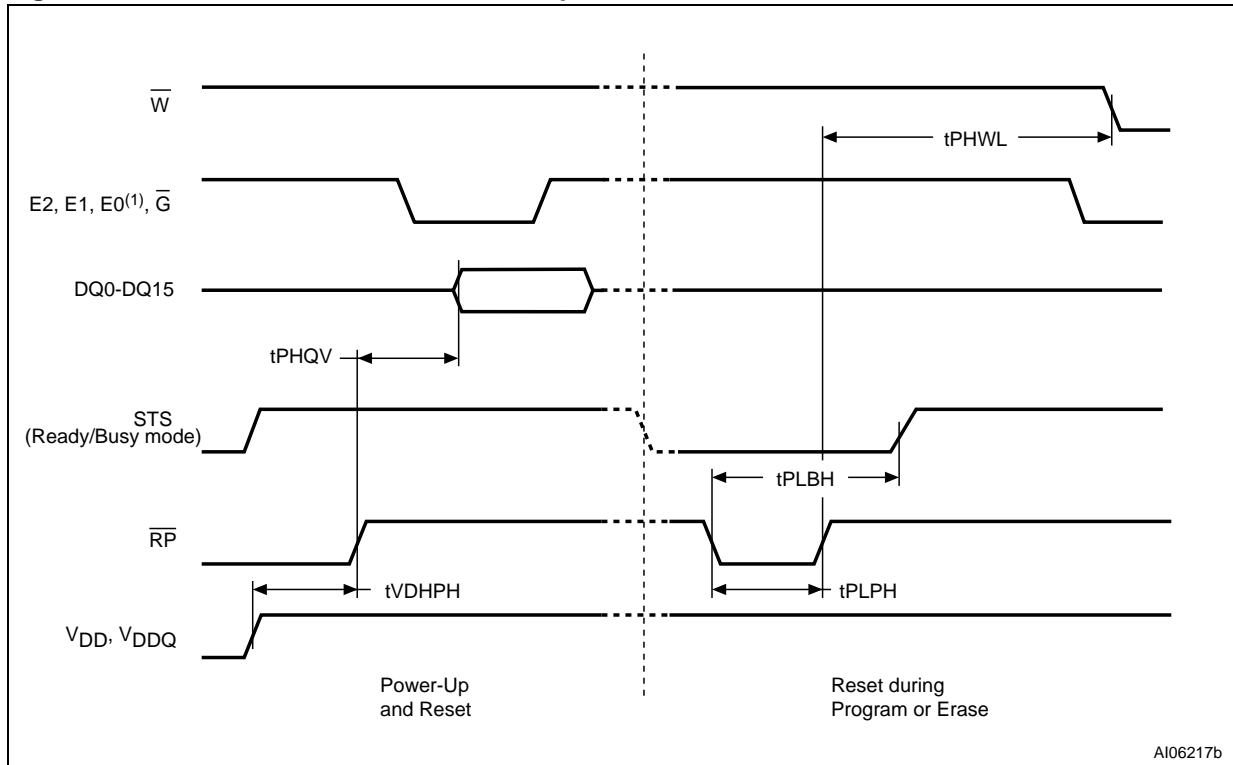
AI06216

Note: 1. V_{IH} = Device Disabled (first edge of E0, E1 or E2), V_{IL} = Device Enabled (first edge of E0, E1 or E2). Refer to Table 2. for more details.

Table 18. Write AC Characteristics, Chip Enable Controlled.

| Symbol | Parameter | | M58LW064D | |
|-------------|---|-----|-----------|------|
| | | | 110 | Unit |
| t_{AVEH} | Address Valid to Chip Enable High | Min | 50 | ns |
| t_{DVEH} | Data Input Valid to Chip Enable High | Min | 50 | ns |
| t_{WLEL} | Write Enable Low to Chip Enable Low | Min | 0 | ns |
| t_{VPHEH} | Program/Erase Enable High to Chip Enable High | Min | 0 | ns |
| t_{EHAX} | Chip Enable High to Address Transition | Min | 5 | ns |
| t_{EHBL} | Chip Enable High to Status/(Ready/Busy) low | Max | 500 | ns |
| t_{EHDX} | Chip Enable High to Input Transition | Min | 5 | ns |
| t_{EHWH} | Chip Enable High to Write Enable High | Min | 0 | ns |
| t_{GHEL} | Output Enable High to Chip Enable Low | Min | 20 | ns |
| t_{EHGL} | Chip Enable High to Output Enable Low | Min | 35 | ns |
| t_{EHEL} | Chip Enable High to Chip Enable Low | Min | 30 | ns |
| t_{ELEH} | Chip Enable Low to Chip Enable High | Min | 70 | ns |

Figure 13. Reset, Power-Down and Power-Up AC Waveform



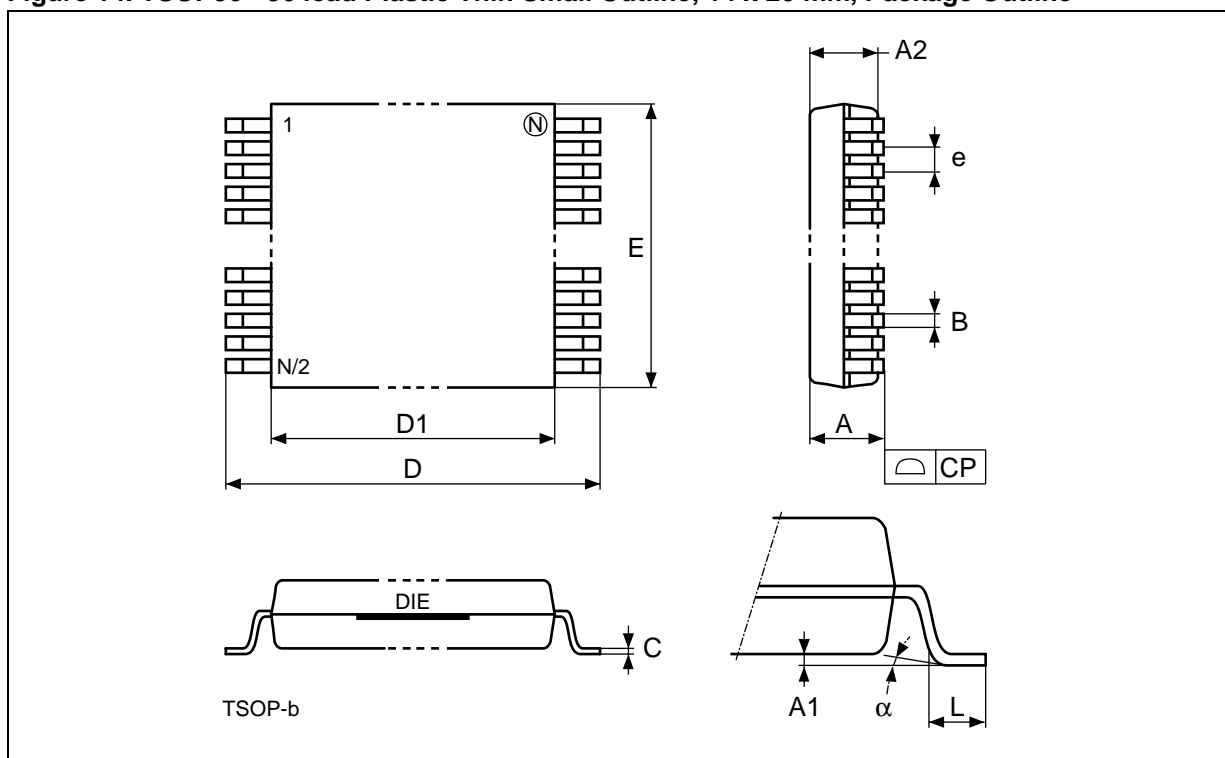
Note: 1. V_{IH} = Device Disabled (first edge of E0, E1 or E2), V_{IL} = Device Enabled (first edge of E0, E1 or E2). Refer to Table 2. for more details.

Table 19. Reset, Power-Down and Power-Up AC Characteristics

| Symbol | Parameter | | M58LW064D | |
|--------------------|--|-----|-----------|------|
| | | | 110 | Unit |
| t _{PHQV} | Reset/Power-Down High to Data Valid | Max | 150 | ns |
| t _{PHWL} | Reset/Power-Down High to Write Enable Low | Max | 1 | μs |
| t _{PLPH} | Reset/Power-Down Low to Reset/Power-Down High | Min | 100 | ns |
| t _{PLBH} | Reset/Power-Down Low to Status/(Ready/Busy) High | Max | 30 | μs |
| t _{VDHPH} | Supply Voltages High to Reset/Power-Down High | Min | 0 | μs |

PACKAGE MECHANICAL

Figure 14. TSOP56 - 56 lead Plastic Thin Small Outline, 14 x 20 mm, Package Outline

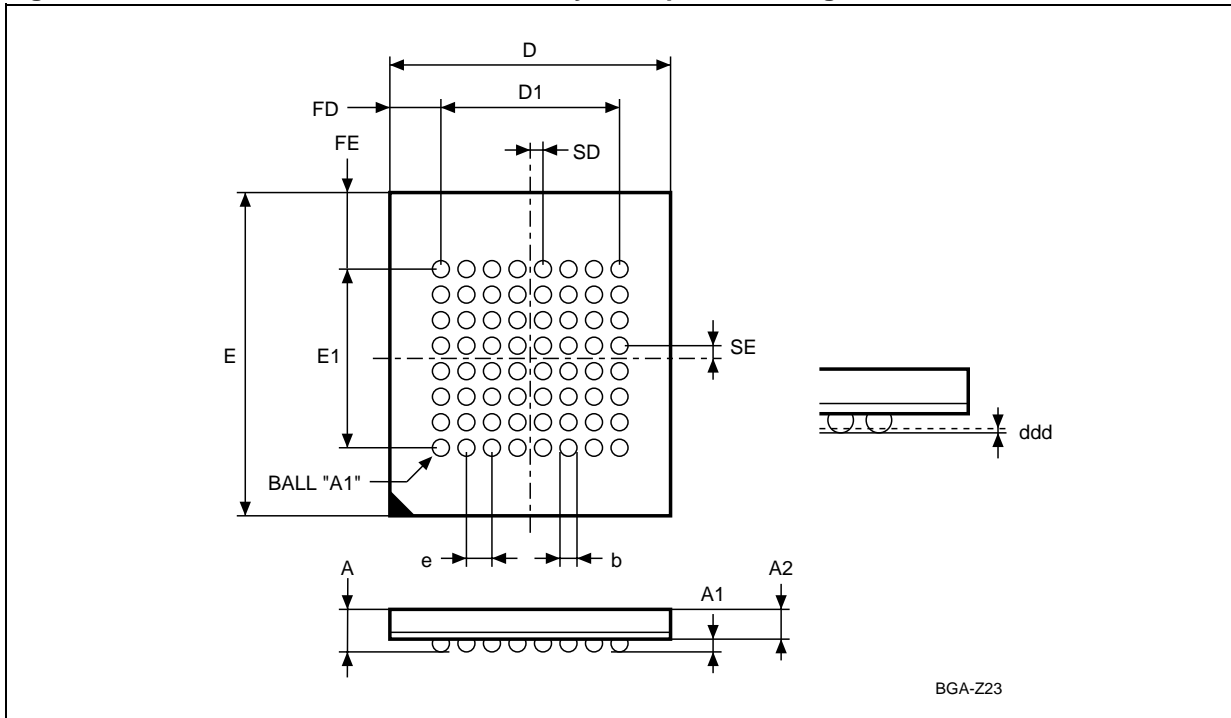


Note: Drawing is not to scale.

Table 20. TSOP56 - 56 lead Plastic Thin Small Outline, 14 x 20 mm, Package Mechanical Data

| Symbol | millimeters | | | inches | | |
|----------|-------------|--------|--------|--------|--------|--------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.200 | | | 0.0472 |
| A1 | 0.100 | 0.050 | 0.150 | 0.0039 | 0.0020 | 0.0059 |
| A2 | 1.000 | 0.950 | 1.050 | 0.0394 | 0.0374 | 0.0413 |
| B | 0.220 | 0.170 | 0.270 | 0.0087 | 0.0067 | 0.0106 |
| C | | 0.100 | 0.210 | | 0.0039 | 0.0083 |
| CP | | | 0.100 | | | 0.0039 |
| D | 20.000 | 19.800 | 20.200 | 0.7874 | 0.7795 | 0.7953 |
| D1 | 18.400 | 18.300 | 18.500 | 0.7244 | 0.7205 | 0.7283 |
| e | 0.500 | – | – | 0.0197 | – | – |
| E | 14.000 | 13.900 | 14.100 | 0.5512 | 0.5472 | 0.5551 |
| L | 0.600 | 0.500 | 0.700 | 0.0236 | 0.0197 | 0.0276 |
| α | 3° | 0° | 5° | 3° | 0° | 5° |
| N | 56 | | | 56 | | |

Figure 15. TBGA64 - 10x13mm, 8 x 8 ball array 1mm pitch, Package Outline



Note: Drawing is not to scale.

Table 21. TBGA64 - 10x13mm, 8 x 8 ball array, 1 mm pitch, Package Mechanical Data

| Symbol | millimeters | | | inches | | |
|--------|-------------|--------|--------|--------|--------|--------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.200 | | | 0.0472 |
| A1 | 0.300 | 0.200 | 0.350 | 0.0118 | 0.0079 | 0.0138 |
| A2 | 0.800 | | | 0.0315 | | |
| b | | 0.350 | 0.500 | | 0.0138 | 0.0197 |
| D | 10.000 | 9.900 | 10.100 | 0.3937 | 0.3898 | 0.3976 |
| D1 | 7.000 | - | - | 0.2756 | - | - |
| ddd | | | 0.100 | | | 0.0039 |
| e | 1.000 | - | - | 0.0394 | - | - |
| E | 13.000 | 12.900 | 13.100 | 0.5118 | 0.5079 | 0.5157 |
| E1 | 7.000 | - | - | 0.2756 | - | - |
| FD | 1.500 | - | - | 0.0591 | - | - |
| FE | 3.000 | - | - | 0.1181 | - | - |
| SD | 0.500 | - | - | 0.0197 | - | - |
| SE | 0.500 | - | - | 0.0197 | - | - |

PART NUMBERING

Table 22. Ordering Information Scheme

Example:

| | M58LW064D | 110 | N | 1 | T |
|--------------------------|--|-----|---|---|---|
| Device Type | M58 | | | | |
| Architecture | L = Page Mode | | | | |
| Operating Voltage | W = $V_{DD} = V_{DDQ} = 2.7V$ to $3.6V$ | | | | |
| Device Function | 064D = 64 Mbit (x8, x16), Uniform Block | | | | |
| Speed | 110 = 110 ns | | | | |
| Package | N = TSOP56: 14 x 20 mm ZA = TBGA64: 10 x 13 mm, 1mm pitch | | | | |
| Temperature Range | 1 = 0 to 70 °C 6 = -40 to 85 °C | | | | |
| Option | Blank = Standard Packing T = Tape & Reel Packing E = Lead-free and RoHS Package, Standard Packing F = Lead-free and RoHS Package, Tape & Reel Packing | | | | |

Note: Devices are shipped from the factory with the memory content bits erased to '1'.

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

APPENDIX A. BLOCK ADDRESS TABLE

Table 23. Block Addresses

| Block Number | Address Range (x8 Bus Width) | Address Range (x16 Bus Width) |
|--------------|------------------------------|-------------------------------|
| 64 | 7E0000h-7FFFFFFh | 3F0000h-3FFFFFFh |
| 63 | 7C0000h-7DFFFFh | 3E0000h-3EFFFFh |
| 62 | 7A0000h-7BFFFFh | 3D0000h-3DFFFFh |
| 61 | 780000h-79FFFFh | 3C0000h-3CFFFFh |
| 60 | 760000h-77FFFFh | 3B0000h-3BFFFFh |
| 59 | 740000h-75FFFFh | 3A0000h-3AFFFFh |
| 58 | 720000h-73FFFFh | 390000h-39FFFFh |
| 57 | 700000h-71FFFFh | 380000h-38FFFFh |
| 56 | 6E0000h-6FFFFFFh | 370000h-37FFFFh |
| 55 | 6C0000h-6DFFFFh | 360000h-36FFFFh |
| 54 | 6A0000h-6BFFFFh | 350000h-35FFFFh |
| 53 | 680000h-69FFFFh | 340000h-34FFFFh |
| 52 | 660000h-67FFFFh | 330000h-33FFFFh |
| 51 | 640000h-65FFFFh | 320000h-32FFFFh |
| 50 | 620000h-63FFFFh | 310000h-31FFFFh |
| 49 | 600000h-61FFFFh | 300000h-30FFFFh |
| 48 | 5E0000h-5FFFFFFh | 2F0000h-2FFFFFFh |
| 47 | 5C0000h-5DFFFFh | 2E0000h-2EFFFFh |
| 46 | 5A0000h-5BFFFFh | 2D0000h-2DFFFFh |
| 45 | 580000h-59FFFFh | 2C0000h-2CFFFFh |
| 44 | 560000h-57FFFFh | 2B0000h-2BFFFFh |
| 43 | 540000h-55FFFFh | 2A0000h-2AFFFFh |
| 42 | 520000h-53FFFFh | 290000h-29FFFFh |
| 41 | 500000h-51FFFFh | 280000h-28FFFFh |
| 40 | 4E0000h-4FFFFFFh | 270000h-27FFFFh |
| 39 | 4C0000h-4DFFFFh | 260000h-26FFFFh |
| 38 | 4A0000h-4BFFFFh | 250000h-25FFFFh |
| 37 | 480000h-49FFFFh | 240000h-24FFFFh |
| 36 | 460000h-47FFFFh | 230000h-23FFFFh |
| 35 | 440000h-45FFFFh | 220000h-22FFFFh |
| 34 | 420000h-43FFFFh | 210000h-21FFFFh |
| 33 | 400000h-41FFFFh | 200000h-20FFFFh |

| Block Number | Address Range (x8 Bus Width) | Address Range (x16 Bus Width) |
|--------------|------------------------------|-------------------------------|
| 32 | 3E0000h-3FFFFFFh | 1F0000h-1FFFFFFh |
| 31 | 3C0000h-3DFFFFh | 1E0000h-1EFFFFh |
| 30 | 3A0000h-3BFFFFh | 1D0000h-1DFFFFh |
| 29 | 380000h-39FFFFh | 1C0000h-1CFFFFh |
| 28 | 360000h-37FFFFh | 1B0000h-1BFFFFh |
| 27 | 340000h-35FFFFh | 1A0000h-1AFFFFh |
| 26 | 320000h-33FFFFh | 190000h-19FFFFh |
| 25 | 300000h-31FFFFh | 180000h-18FFFFh |
| 24 | 2E0000h-2FFFFFFh | 170000h-17FFFFh |
| 23 | 2C0000h-2DFFFFh | 160000h-16FFFFh |
| 22 | 2A0000h-2BFFFFh | 150000h-15FFFFh |
| 21 | 280000h-29FFFFh | 140000h-14FFFFh |
| 20 | 260000h-27FFFFh | 130000h-13FFFFh |
| 19 | 240000h-25FFFFh | 120000h-12FFFFh |
| 18 | 220000h-23FFFFh | 110000h-11FFFFh |
| 17 | 200000h-21FFFFh | 100000h-10FFFFh |
| 16 | 1E0000h-1FFFFFFh | 0F0000h-0FFFFFFh |
| 15 | 1C0000h-1DFFFFh | 0E0000h-0EFFFFh |
| 14 | 1A0000h-1BFFFFh | 0D0000h-0DFFFFh |
| 13 | 180000h-19FFFFh | 0C0000h-0CFFFFh |
| 12 | 160000h-17FFFFh | 0B0000h-0BFFFFh |
| 11 | 140000h-15FFFFh | 0A0000h-0AFFFFh |
| 10 | 120000h-13FFFFh | 090000h-09FFFFh |
| 9 | 100000h-11FFFFh | 080000h-08FFFFh |
| 8 | 0E0000h-0FFFFFFh | 070000h-07FFFFh |
| 7 | 0C0000h-0DFFFFh | 060000h-06FFFFh |
| 6 | 0A0000h-0BFFFFh | 050000h-05FFFFh |
| 5 | 080000h-09FFFFh | 040000h-04FFFFh |
| 4 | 060000h-07FFFFh | 030000h-03FFFFh |
| 3 | 040000h-05FFFFh | 020000h-02FFFFh |
| 2 | 020000h-03FFFFh | 010000h-01FFFFh |
| 1 | 000000h-01FFFFh | 000000h-00FFFFh |

APPENDIX B. COMMON FLASH INTERFACE - CFI

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the de-

vice, enabling the software to upgrade itself when necessary.

When the CFI Query Command (RCFI) is issued the device enters CFI Query mode and the data structure is read from the memory. Tables 24, 25, 26, 27, 28 and 29 show the addresses used to retrieve the data.

Table 24. Query Structure Overview

| Address | | Sub-section Name | Description |
|---------------------|-------------------|---|---|
| x16 | x8 ⁽⁴⁾ | | |
| 0000h | 00h | | Manufacturer Code |
| 0001h | 02h | | Device Code |
| 0010h | 20h | CFI Query Identification String | Command set ID and algorithm data offset |
| 001Bh | 36h | System Interface Information | Device timing and voltage information |
| 0027h | 4Eh | Device Geometry Definition | Flash memory layout |
| P(h) ⁽¹⁾ | | Primary Algorithm-specific Extended Query Table | Additional information specific to the Primary Algorithm (optional) |
| A(h) ⁽²⁾ | | Alternate Algorithm-specific Extended Query Table | Additional information specific to the Alternate Algorithm (optional) |
| (SBA+02)h | | Block Status Register | Block-related Information |

Note: 1. Offset 15h defines P which points to the Primary Algorithm Extended Query Address Table.
 2. Offset 19h defines A which points to the Alternate Algorithm Extended Query Address Table.
 3. SBA is the Start Base Address for each block.
 4. In x8 mode, A0 must be set to V_{IL}, otherwise 00h will be output.

Table 25. CFI - Query Address and Data Output

| Address | | Data | | Description |
|----------------------|-------------------|------|-----|--|
| x16 | x8 ⁽³⁾ | | | |
| 0010h | 20h | 51h | "Q" | 51h; "Q" Query ASCII String 52h; "R" 59h; "Y" |
| 0011h | 22h | 52h | "R" | |
| 0012h | 24h | 59h | "Y" | |
| 0013h | 26h | 01h | | Primary Vendor: Command Set and Control Interface ID Code |
| 0014h | 28h | 00h | | |
| 0015h | 2Ah | 31h | | Primary algorithm extended Query Address Table: P(h) |
| 0016h | 2Ch | 00h | | |
| 0017h | 2Eh | 00h | | Alternate Vendor: Command Set and Control Interface ID Code |
| 0018h | 30h | 00h | | |
| 0019h | 32h | 00h | | Alternate Algorithm Extended Query address Table |
| 001Ah ⁽²⁾ | 34h | 00h | | |

Note: 1. Query Data are always presented on DQ7-DQ0. DQ15-DQ8 are set to '0'.
 2. Offset 19h defines A which points to the Alternate Algorithm Extended Query Address Table.
 3. In x8 mode, A0 must be set to V_{IL}, otherwise 00h will be output.

Table 26. CFI - Device Voltage and Timing Specification

| Address | | Data | Description |
|---------|-------------------|--------------------|---|
| x16 | x8 ⁽⁴⁾ | | |
| 001Bh | 36h | 27h ⁽¹⁾ | V _{DD} Min, 2.7V |
| 001Ch | 38h | 36h ⁽¹⁾ | V _{DD} max, 3.6V |
| 001Dh | 3Ah | 00h ⁽²⁾ | V _{PP} min – Not Available |
| 001Eh | 3Ch | 00h ⁽²⁾ | V _{PP} max – Not Available |
| 001Fh | 3Eh | 04h | 2 ⁿ μs typical time-out for Word, DWord prog – Not Available |
| 0020h | 40h | 08h | 2 ⁿ μs, typical time-out for max buffer write |
| 0021h | 42h | 0Ah | 2 ⁿ ms, typical time-out for Erase Block |
| 0022h | 44h | 00h ⁽³⁾ | 2 ⁿ ms, typical time-out for chip erase – Not Available |
| 0023h | 46h | 04h | 2 ⁿ x typical for Word Dword time-out max – Not Available |
| 0024h | 48h | 04h | 2 ⁿ x typical for buffer write time-out max |
| 0025h | 4Ah | 04h | 2 ⁿ x typical for individual block erase time-out maximum |
| 0026h | 4Ch | 00h ⁽³⁾ | 2 ⁿ x typical for chip erase max time-out – Not Available |

Note: 1. Bits are coded in Binary Code Decimal, bit7 to bit4 are scaled in Volts and bit3 to bit0 in mV.
 2. Bit7 to bit4 are coded in Hexadecimal and scaled in Volts while bit3 to bit0 are in Binary Code Decimal and scaled in 100mV.
 3. Not supported.
 4. In x8 mode, A0 must be set to V_{IL}, otherwise 00h will be output.

Table 27. Device Geometry Definition

| Address | | Data | Description |
|---------|-------------------|------|--|
| x16 | x8 ⁽¹⁾ | | |
| 0027h | 4Eh | 17h | n where 2 ⁿ is number of bytes memory Size |
| 0028h | 50h | 02h | Device Interface |
| 0029h | 52h | 00h | Organization Sync./Async. |
| 002Ah | 54h | 05h | Maximum number of bytes in Write Buffer, 2 ⁿ |
| 002Bh | 56h | 00h | |
| 002Ch | 58h | 01h | Bit7-0 = number of Erase Block Regions in device |
| 002Dh | 5Ah | 3Fh | Number (n-1) of Erase Blocks of identical size; n=64 |
| 002Eh | 5Ch | 00h | |
| 002Fh | 5Eh | 00h | Erase Block Region Information x 256 bytes per Erase block (128K bytes) |
| 0030h | 60h | 02h | |

Note: 1. In x8 mode, A0 must be set to V_{IL}, otherwise 00h will be output.

Table 28. Block Status Register

| Address | Data | | Selected Block Information |
|--------------------------|--------|---|--|
| (BA+2)h ^(1,2) | bit0 | 0 | Block Unprotected |
| | | 1 | Block Protected |
| | bit1 | 0 | Last erase operation ended successfully ⁽³⁾ |
| | | 1 | Last erase operation not ended successfully ⁽³⁾ |
| | bit7-2 | 0 | Reserved for future features |

Note: 1. BA specifies the block address location, A22-A17.
 2. In x8 mode, A0 must be set to V_{IL}, otherwise 00h will be output.
 3. Not Supported.

Table 29. Extended Query information

| Address | | | Data (Hex) | | Description |
|---------|-------|-------------------|------------|-----|--|
| offset | x16 | x8 ⁽²⁾ | | | |
| (P)h | 0031h | 62h | 50h | "P" | Query ASCII string - Extended Table |
| (P+1)h | 0032h | 64h | 52h | "R" | |
| (P+2)h | 0033h | 66h | 49h | "I" | |
| (P+3)h | 0034h | 68h | 31h | | Major version number |
| (P+4)h | 0035h | 6Ah | 31h | | Minor version number |
| (P+5)h | 0036h | 6Ch | CEh | | Optional Feature: (1=yes, 0=no) bit0, Chip Erase Supported (0=no) bit1, Suspend Erase Supported (1=yes) bit2, Suspend Program Supported (1=yes) bit3, Protect/Unprotect Supported (1=yes) bit4, Queue Erase Supported (0=no) bit5, Instant Individual Block locking (0=no) bit6, Protection bits supported (1=yes) bit7, Page Read supported (1=yes) bit 8, Synchronous Read supported (0=no) bits 9 to 31 reserved for future use |
| (P+6)h | 0037h | 6Eh | 00h | | |
| (P+7)h | 0038h | 70h | 00h | | |
| (P+8)h | 0039h | 72h | 00h | | |
| (P+9)h | 003Ah | 74h | 01h | | Function allowed after Suspend: Program allowed after Erase Suspend (1=yes) Bit 7-1 reserved for future use |
| (P+A)h | 003Bh | 76h | 01h | | Block Status Register bit0, Block Protect-Bit status active (1=yes) bit1, Block Lock-Down Bit status (not available) bits 2 to 15 reserved for future use |
| (P+B)h | 003Ch | 78h | 00h | | |
| (P+C)h | 003Dh | 7Ah | 33h | | V _{DD} OPTIMUM Program/Erase voltage conditions |
| (P+D)h | 003Eh | 7Ch | 00h | | V _{PP} OPTIMUM Program/Erase voltage conditions |
| (P+E)h | 003Fh | 7Eh | 01h | | OTP protection: No. of protection register fields |
| (P+F)h | 0040h | 80h | 80h | | Protection Register's start address, least significant bits |
| (P+10)h | 0041h | 82h | 00h | | Protection Register's start address, most significant bits |
| (P+11)h | 0042h | 84h | 03h | | n where 2 ⁿ is number of factory reprogrammed bytes |
| (P+12)h | 0043h | 86h | 03h | | n where 2 ⁿ is number of user programmable bytes |

M58LW064D

| Address | | | Data (Hex) | Description |
|---------|-------|-------------------|-------------------------|--|
| offset | x16 | x8 ⁽²⁾ | | |
| (P+13)h | 0044h | 88h | 03h | Page Read: 2 ⁿ Bytes (n = bits 0-7) |
| (P+14)h | 0045h | 8Ah | 00h | Synchronous mode configuration fields |
| (P+15)h | 0046h | 8Ch | Reserved for future use | |

Note: 1. Bit7 to bit4 are coded in Hexadecimal and scaled in Volt while bit3 to bit0 are in Binary Code Decimal and scaled in mV.
2. In x8 mode, A0 must be set to V_{IL}, otherwise 00h will be output.

APPENDIX C. FLOW CHARTS

Figure 16. Write to Buffer and Program Flowchart and Pseudo Code

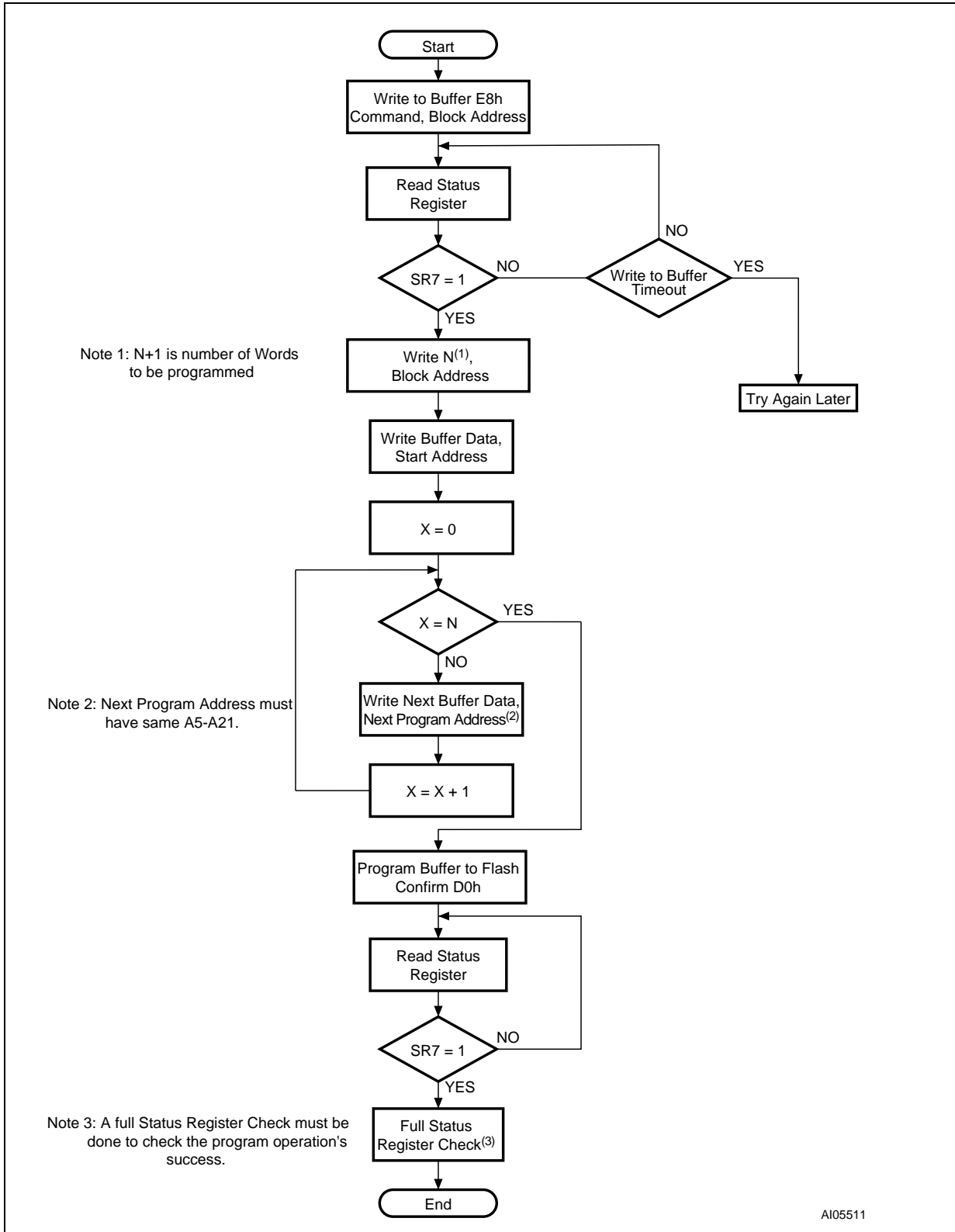


Figure 17. Program Suspend & Resume Flowchart and Pseudo Code

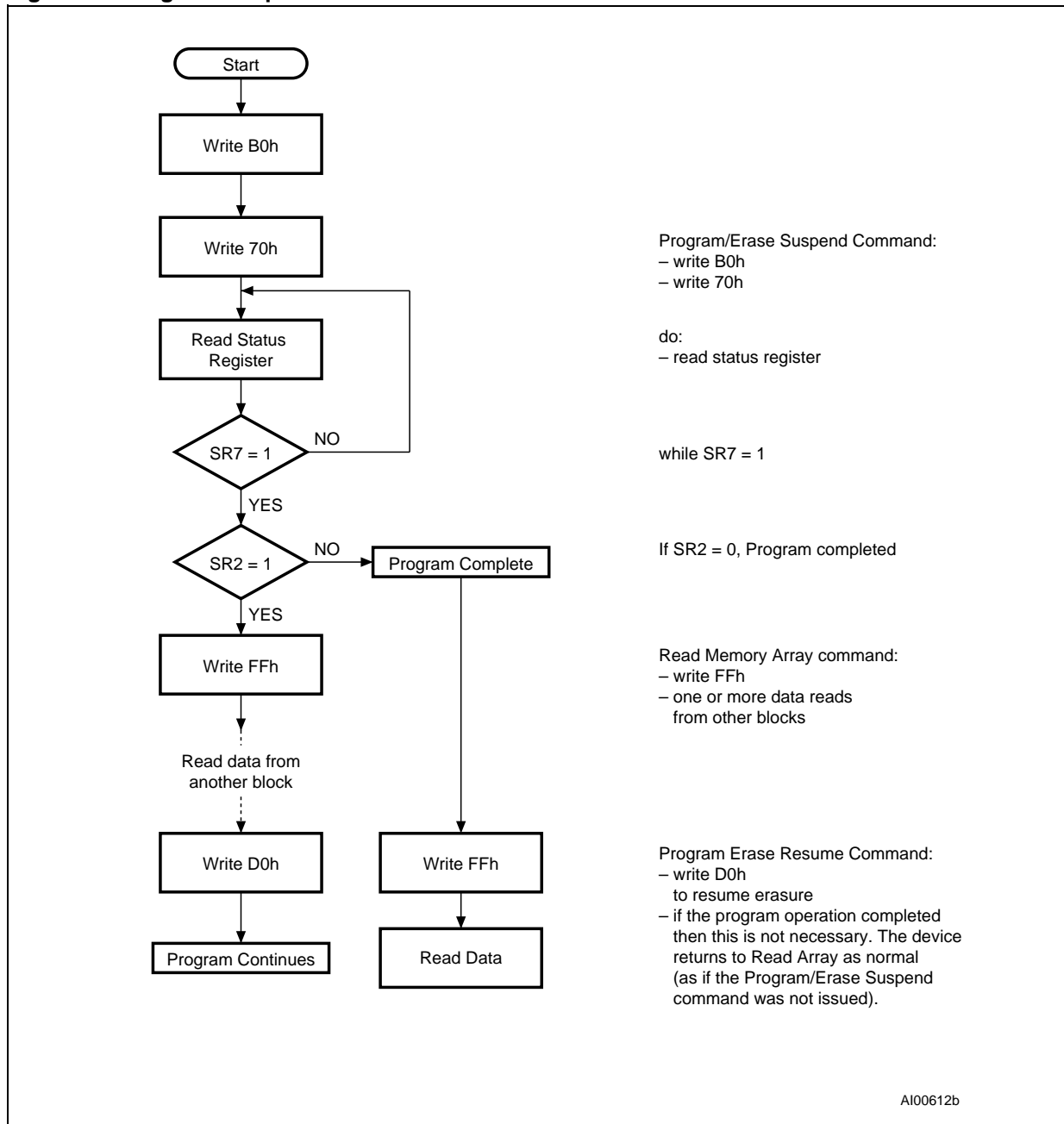
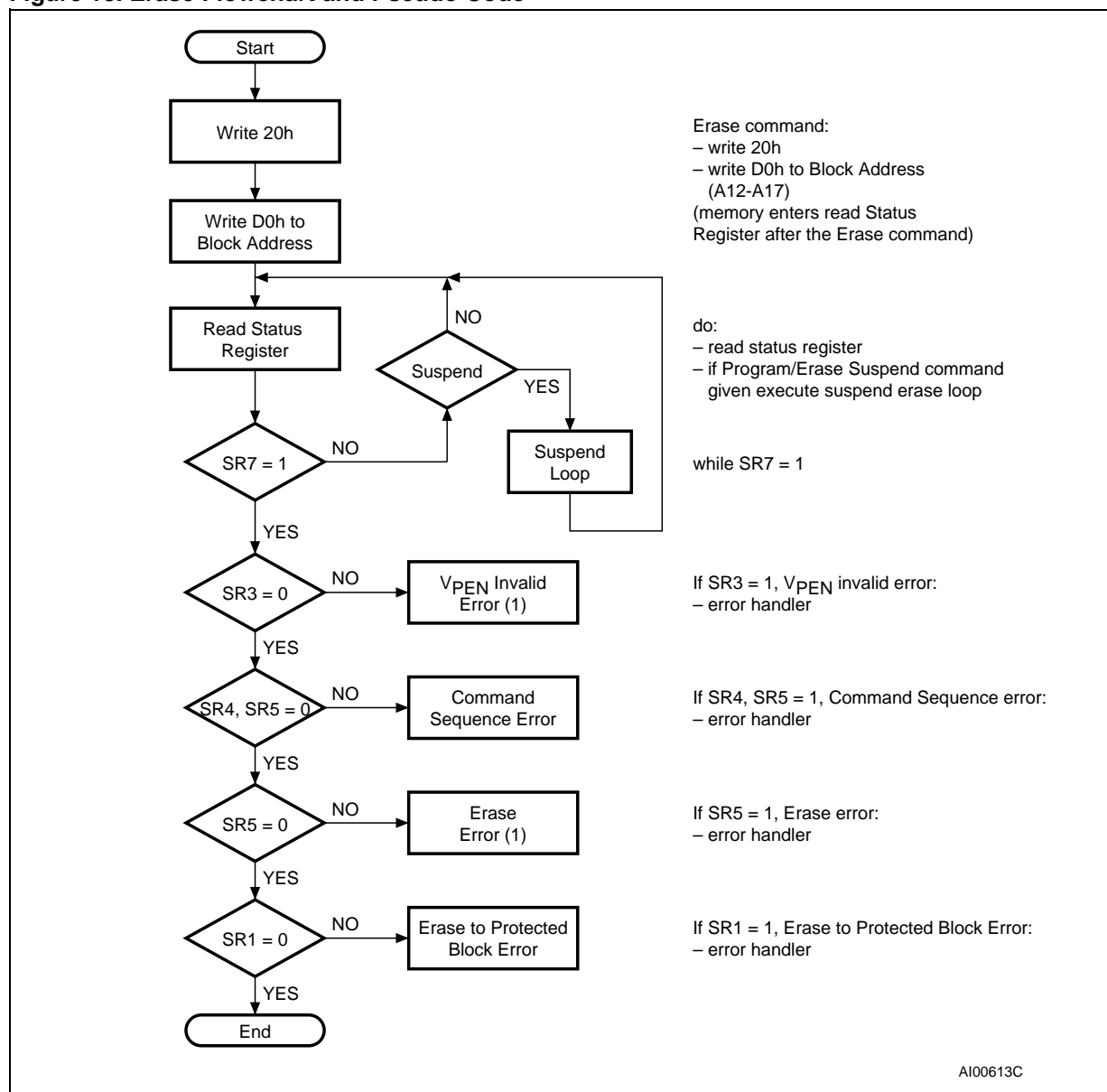


Figure 18. Erase Flowchart and Pseudo Code



Note: 1. If an error is found, the Status Register must be cleared (Clear Status Register Command) before further Program or Erase operations.

Figure 19. Erase Suspend & Resume Flowchart and Pseudo Code

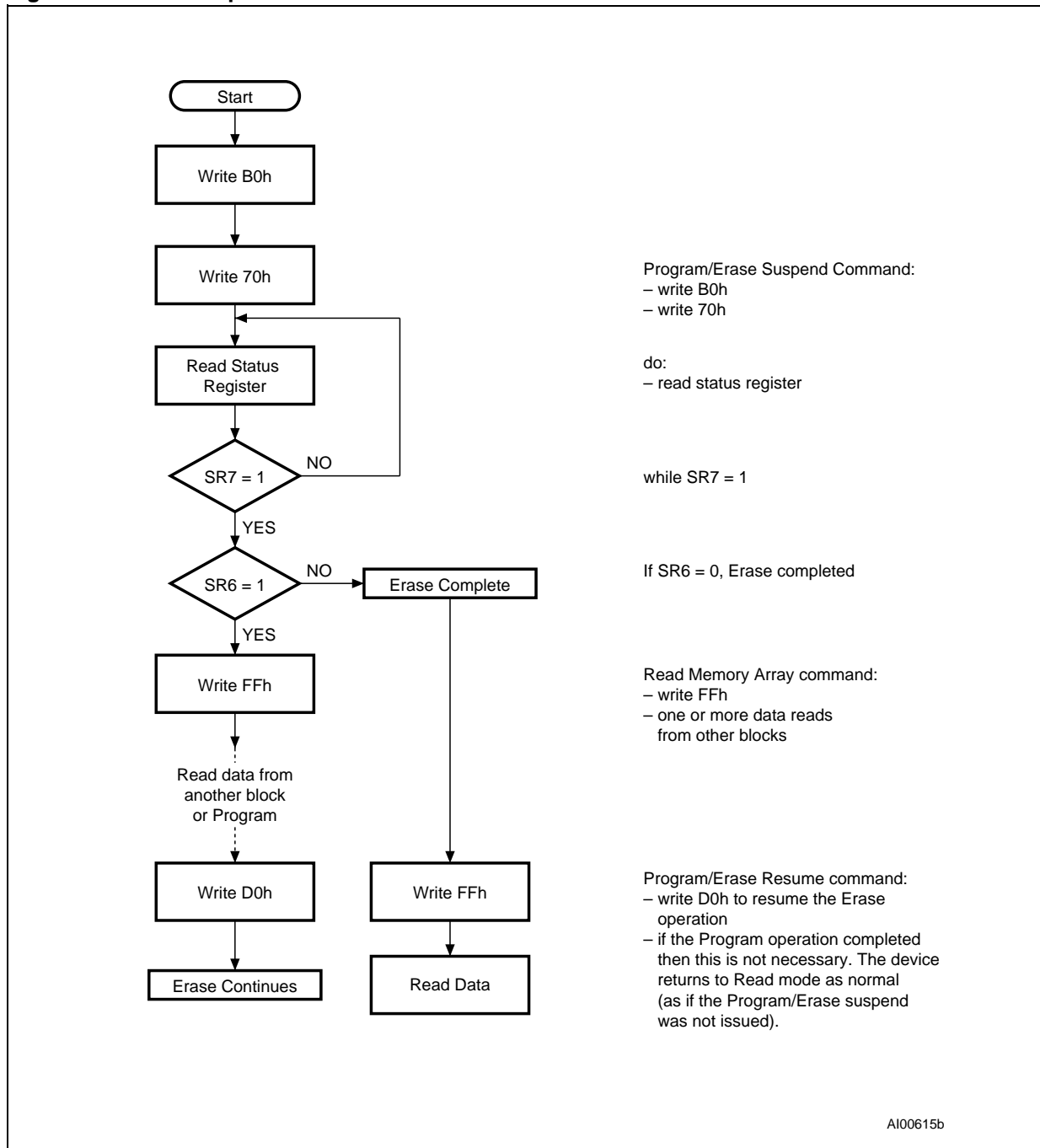


Figure 20. Block Protect Flowchart and Pseudo Code

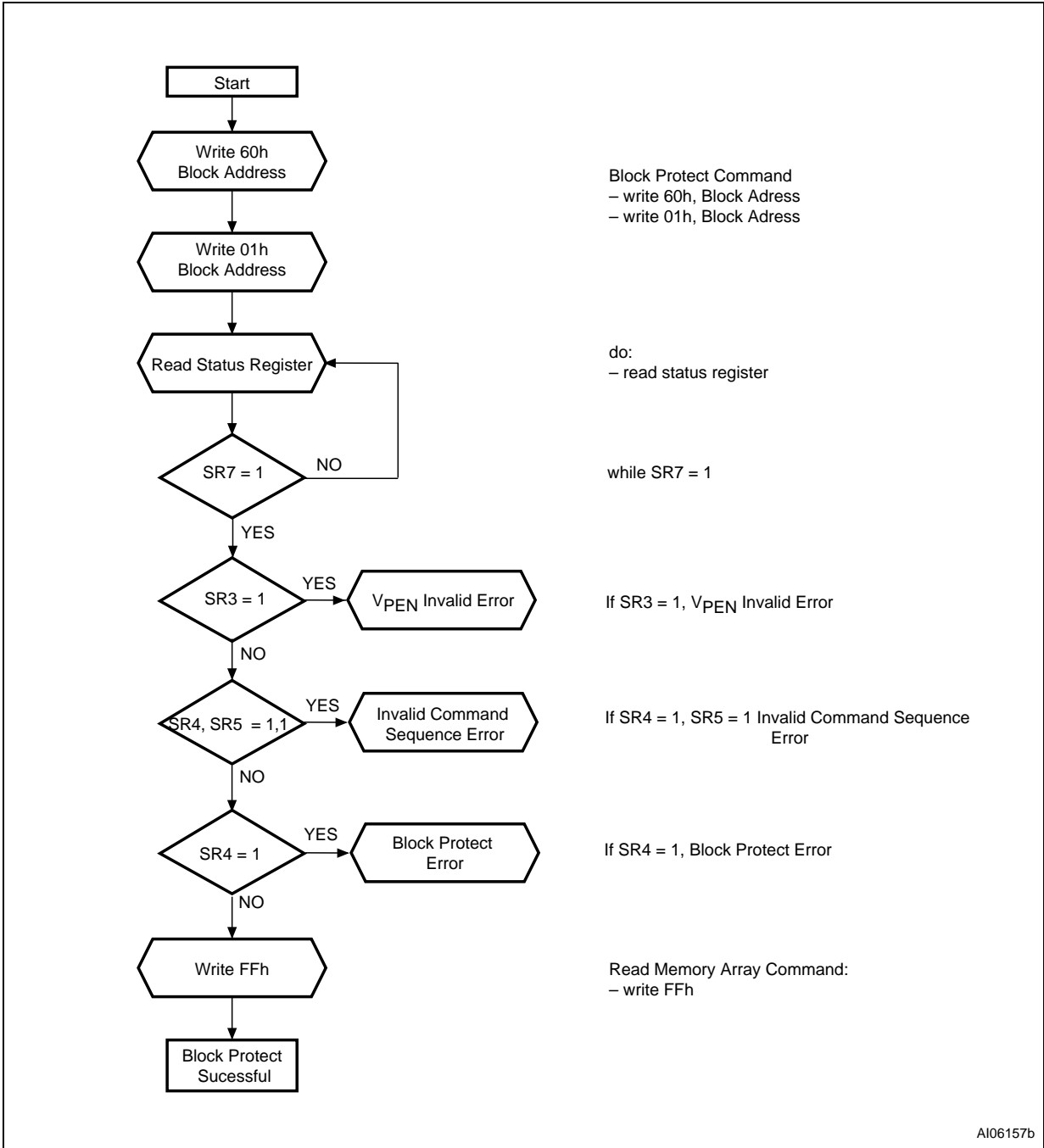


Figure 21. Blocks Unprotect Flowchart and Pseudo Code

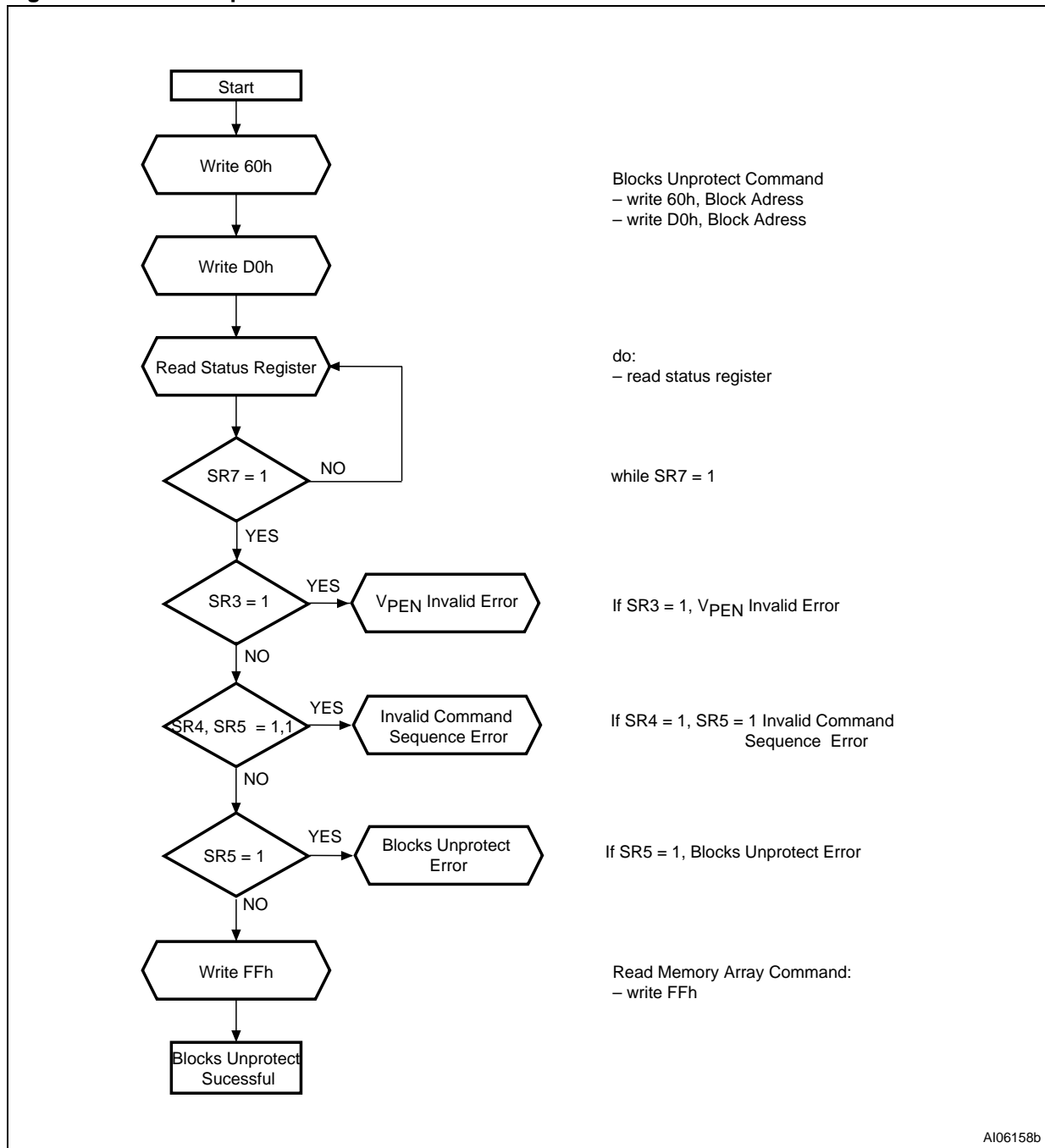
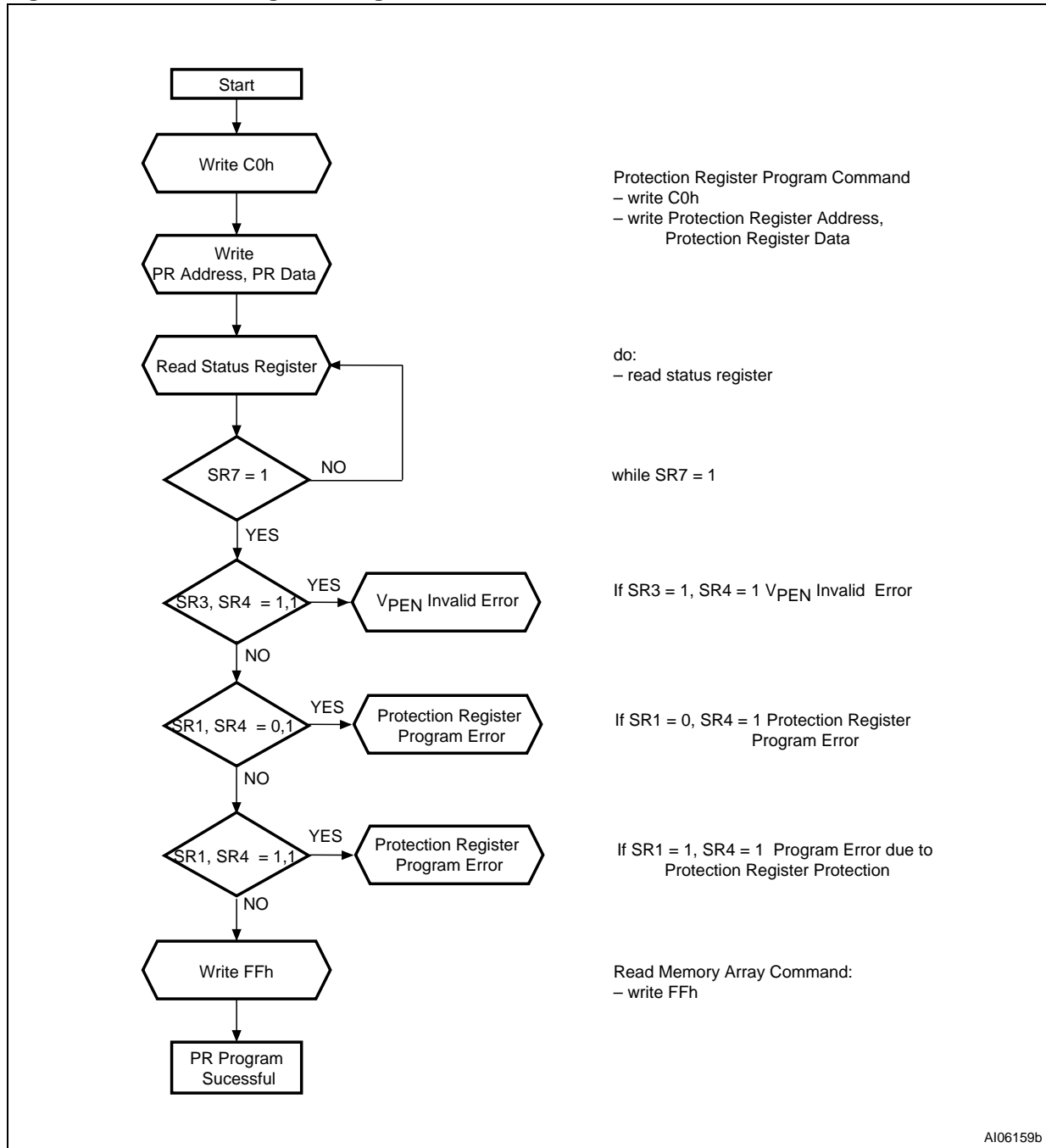


Figure 22. Protection Register Program Flowchart and Pseudo Code



Note: PR = Protection Register

Figure 23. Command Interface and Program Erase Controller Flowchart (a)

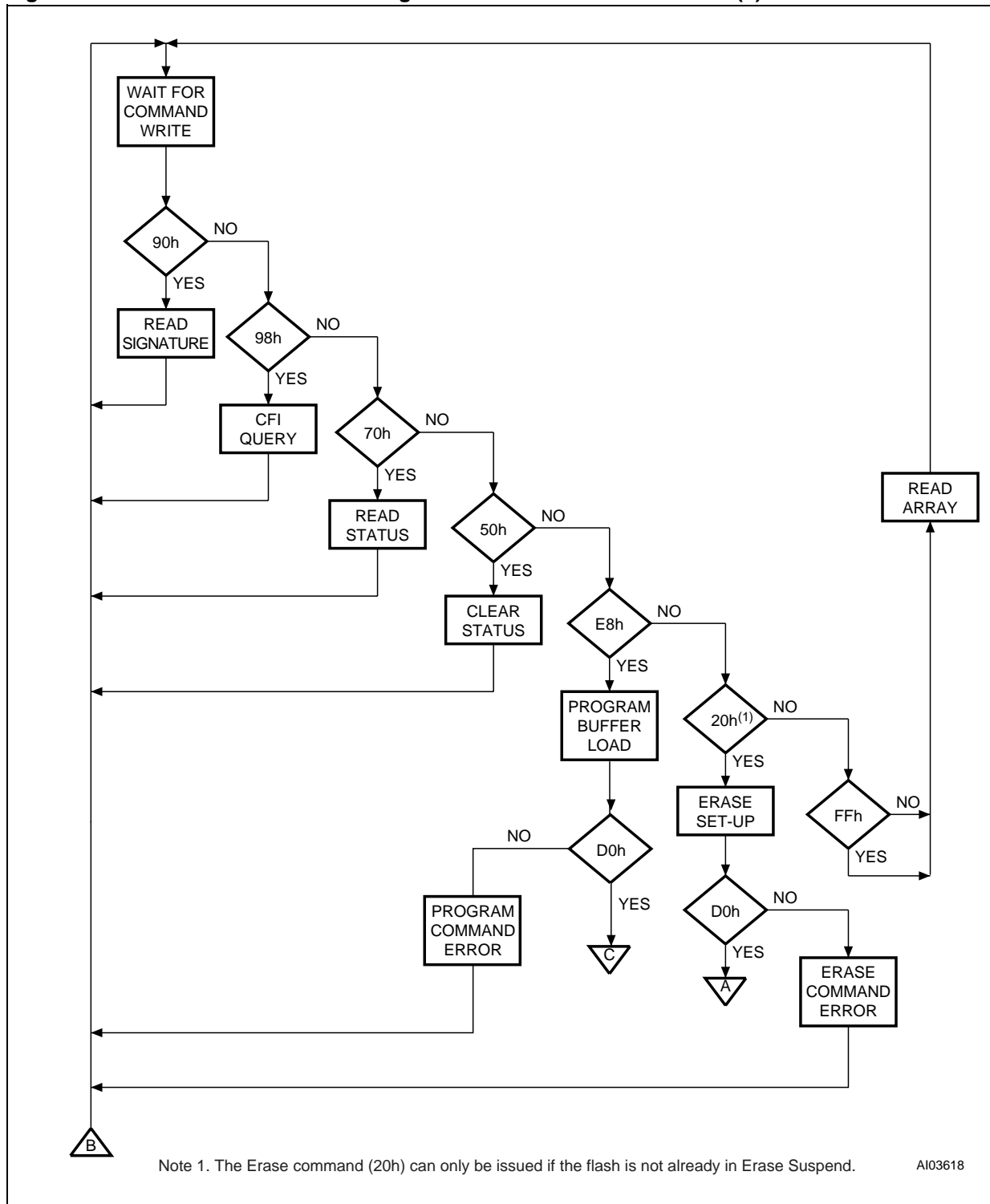
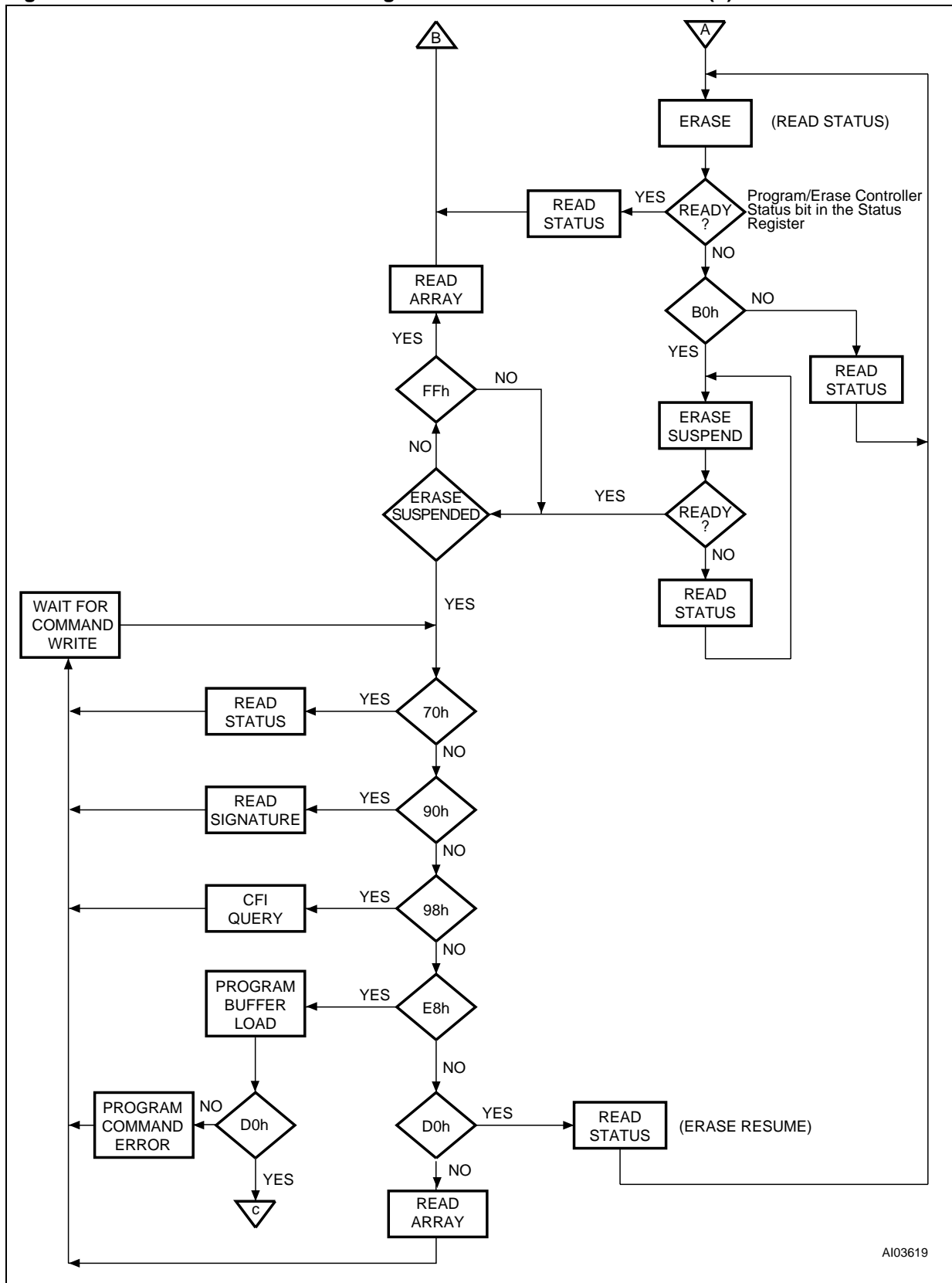


Figure 24. Command Interface and Program Erase Controller Flowchart (b)



AI03619

REVISION HISTORY

Table 30. Document Revision History

| Date | Version | Revision Details |
|-------------|---------|---|
| 08-Nov-2001 | -01 | First Issue (Data Brief) |
| 01-Feb-2002 | -02 | x8 Bus Width added, Speed Class modified, Signal Names and Connections modified |
| 09-Apr-2002 | -03 | Document expanded to full Product Preview |
| 16-Jul-2002 | 3.1 | Revision numbering modified: a minor revision will be indicated by incrementing the digit after the dot, and a major revision, by incrementing the digit before the dot (revision version 03 becomes 3.0). t_{WHDX} and t_{WHAX} changed in Table 17. , "Write AC Characteristics". |
| 06-Aug-2002 | 4.0 | Device Code changed and Effective Programming Time modified. V_{DDQ} range modified (in particular in Tables 12 and 22 , and V_{DDQ} removed from note 1 below Table 9.). In Table 9. , Block Erase Time and Program Write Buffer Time parameters modified. Figure 2. , Logic Diagram , modified. V_{DD} , V_{DDQ} , V_{SS} and V_{SSQ} pin descriptions modified. Document status changed from Product Preview to Preliminary Data. |
| 14-Oct-2002 | 4.1 | A0 Address Line described separately from others (A1-A22) in Table 1. and in "SIGNAL DESCRIPTIONS" paragraph. Address Lines modified in Table 3. , Bus Operations . Byte signal added to Figure 9. , Random Read AC Waveforms , timings t_{ELBL} , t_{BLQV} and t_{BLQZ} added to Table 15. , Random Read AC Characteristics ., timings t_{AVLH} and t_{ELLH} removed from Table 18. , Write AC Characteristics , Chip Enable Controlled . "Write 70h" removed from flowchart Figures 17 and 19 . Table 3. , Bus Operations , clarified. REVISION HISTORY moved to after appendices. |
| 16-Dec-2002 | 4.2 | Table 9. , Program, Erase Times and Program Erase Endurance Cycles modified. Table 6. , Read Electronic Signature clarified. Certain DU connections changed to NC in Figure 4. , TBGA64 Connections (Top view through package) . x8 Address modified in Table 24. , Query Structure Overview . Note regarding A0 value in x8 mode added to all CFI Tables. Block Protect setup command address modified in Table 4. , Commands . Data and Descriptions clarified in CFI Table 29. , Extended Query information . I_{OSC} parameter added to Absolute Maximum Ratings table. I_{DD} and V_{LKO} clarified and I_{DDO} and V_{PENH} parameters added to DC Characteristics table. t_{PHWL} parameter added to Reset, Power-Down and Power-Up AC Waveforms figure and Characteristics table. |
| 16-Apr-2003 | 5.0 | Document promoted to full datasheet. Summary Description clarified, Bus Operations clarified, Read Modes section added, Status Register bit nomenclature modified, V_{PEN} Invalid Error clarified in Flowcharts. Lead-free packing options added to Ordering Information Scheme. |
| 02-Sep-2004 | 6.0 | Lead-Free package options mentioned in FEATURES SUMMARY and SUMMARY DESCRIPTION . T_{LEAD} and note 1 added to Table 11. , Absolute Maximum Ratings . TSOP56 and TBGA64 package specifications updated (see Figure 14. , Table 20. , Figure 15. and Table 21.) Document moved to new template. |

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