PEEL™ 22CV10A-7/-10/-15/-25
CMOS Programmable Electrically Erasable Logic Device

Features

High Speed/Low Power
- Speeds ranging from 7ns to 25ns
- Power as low as 30mA at 25MHz

Electrically Erasable Technology
- Superior factory testing
- Reprogrammable in plastic package
- Reduces retrofit and development costs

Development/Programmer Support
- Third party software and programmers
- Anachip PLACE Development Software

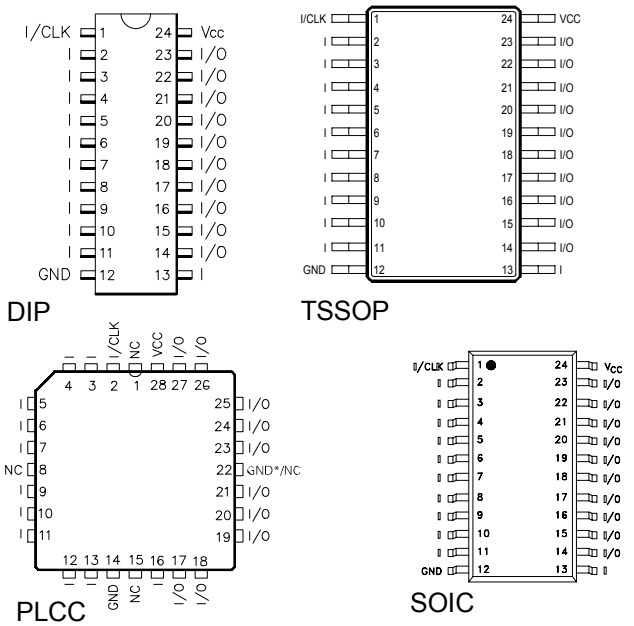
Architectural Flexibility
- 132 product term X 44 input AND array
- Up to 22 inputs and 10 outputs
- Up to 12 configurations per macrocell
- Synchronous preset, asynchronous clear
- Independent output enables
- 24-pin DIP/SOIC/TSSOP and 28-pin PLCC

Application Versatility
- Replaces random logic
- Pin and JEDEC compatible with 22V10
- Enhanced Architecture fits more logic than ordinary PLDs

General Description

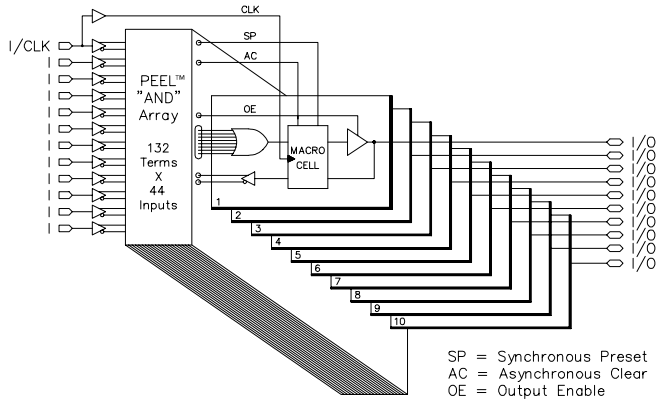
The PEEL™22CV10A is a Programmable Electrically Erasable Logic (PEEL™) device providing an attractive alternative to ordinary PLDs. The PEEL™22CV10A offers the performance, flexibility, ease of design and production practicality needed by logic designers today. The PEEL™22CV10A is available in 24-pin DIP, SOIC, TSSOP and 28-pin PLCC packages (see Figure 1), with speeds ranging from 7ns to 25ns and with power consumption as low as 30mA. EE-reprogrammability provides the conve- nience of instant reprogramming for development and a reusable production inventory, minimizing the impact of programming changes or errors. EE-reprogrammability also improves factory testability, thus ensuring the highest quality possible. The PEEL™22CV10A is JEDEC file compatible with standard 22V10 PLDs. Eight additional configurations per macrocell (a total of 12) are also available by using the "+" software/programming option (i.e., 22CV10A+ & 22CV10A++). The additional macrocell configurations allow more logic to be put into every design. Programming and development support for the PEEL™22CV10A are provided by popular third-party programmers and development software. Anachip also offers free PLACE development software.

Figure 1. Pin Configuration



*Optional extra ground pin for -7/I-7 speed grade.

Figure 2. Block Diagram



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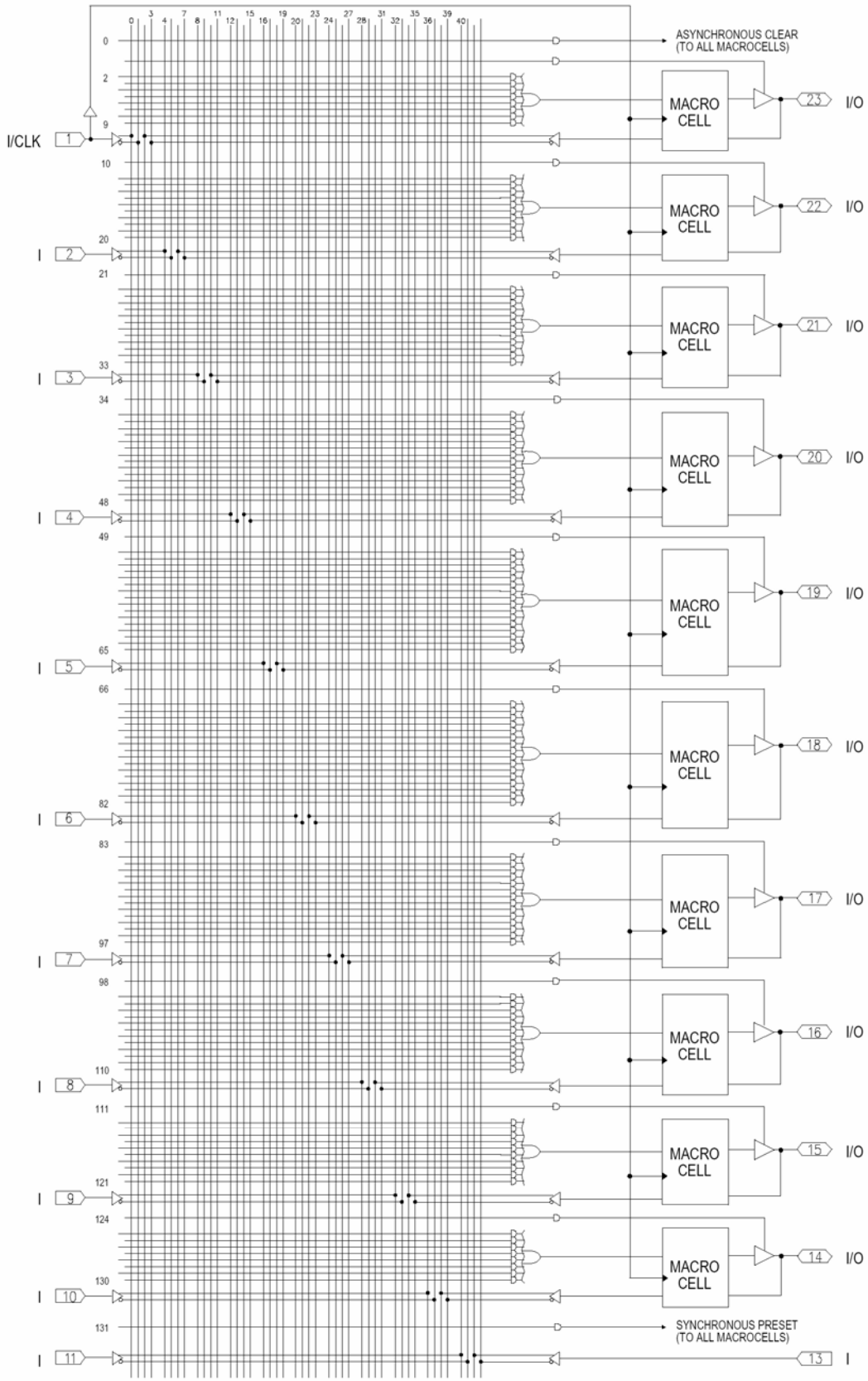


Figure 3. PEEL™22CV10A Logic Array Diagram

Function Description

The PEEL™22CV10A implements logic functions as sum-of-products expressions in a programmable-AND/ fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL™22CV10A architecture is illustrated in the block diagram of Figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure, the PEEL™22CV10A can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 4 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions with either active-high or active-low polarity.

AND/OR Logic Array

The programmable AND array of the PEEL™22CV10A (shown in Figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

24 input lines carry the true and complement
of the signals applied to the 12 input pins
20 additional lines carry the true and complement
values of feedback or input signals from
the 10 I/Os

132 product terms:

120 product terms (arranged in 2 groups of 8,
10, 12, 14 and 16) used to form logical sums
10 output enable terms (one for each I/O)
1 global synchronous present term
1 global asynchronous clear term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE, and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a “don’t care” state exists and that term will always be TRUE. When programming the PEEL™22CV10A, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is then configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL™ device programmers automatically program the connections on unused product terms so that they will have no effect on the output function.)

Variable Product Term Distribution

The PEEL™22CV10A provides 120 product terms to drive the 10 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14 and 16 to form logical sums (see Figure 3). This distribution allows optimum use of device re-sources.

Programmable I/O Macrocell

The output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL™22CV10A to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in Figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the two EEPROM bits controlling these multiplexers (refer to Table 1). These bits determine output polarity and output type (registered or non-registered). Equivalent circuits for the four macro-cell configurations are illustrated in Figure 5.

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the glo- bal preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output

enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

When configuring an I/O macrocell to implement a registered function (configurations 1 and 2 in Figure 5), the Q output of the flip-flop drives the feedback term. When configuring an I/O macrocell to implement a combinatorial function (configurations 3 and 4 in Figure 5), the feedback signal is taken from the I/O pin. In this case, the pin can be used as a dedicated input or a bi-directional I/O. (Refer also to Table 1.)

Additional Macro Cell Configurations

Besides the standard four-configuration macrocell shown in Figure 5, each PEEL™22CV10A provides an additional eight configurations that can be used to increase design flexibility. The configurations are the same as provided by the PEEL™18CV8 and PEEL™22CV10AZ. However, to maintain JEDEC file compatibility with standard 22V10 PLDs the additional configurations can only be utilized by specifying the PEEL™22CV10A+ and PEEL22CV10A++ for logic assembly and programming. To reference these additional configurations please refer to the specifications at the end of this data sheet.

Design Security

The PEEL™22CV10A provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step after the device has been programmed. Once the security bit is set, it is impossible to verify (read) or program the PEEL™ until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 24-bit code to be programmed into the PEEL™22CV10A if the PEEL™22CV10A+ software option is used. Also, the signature word feature allows a 64-bit code to be programmed into the PEEL™22CV10A if the PEEL™22CV10A++ software option is used. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

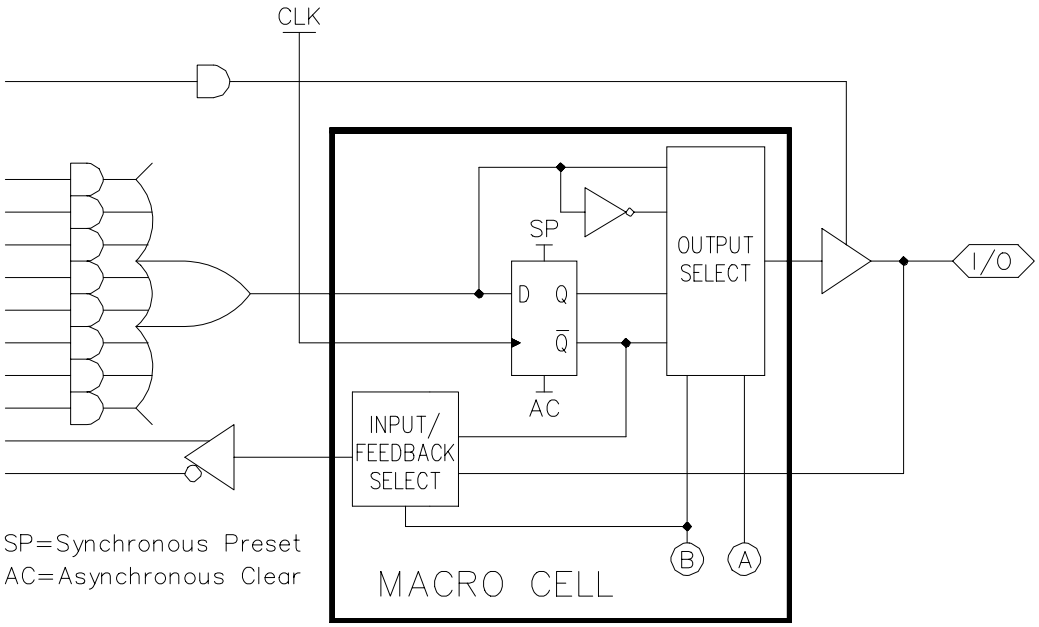


Figure 4. Block Diagram of the PEEL™ 22CV10A I/O Macrocell.

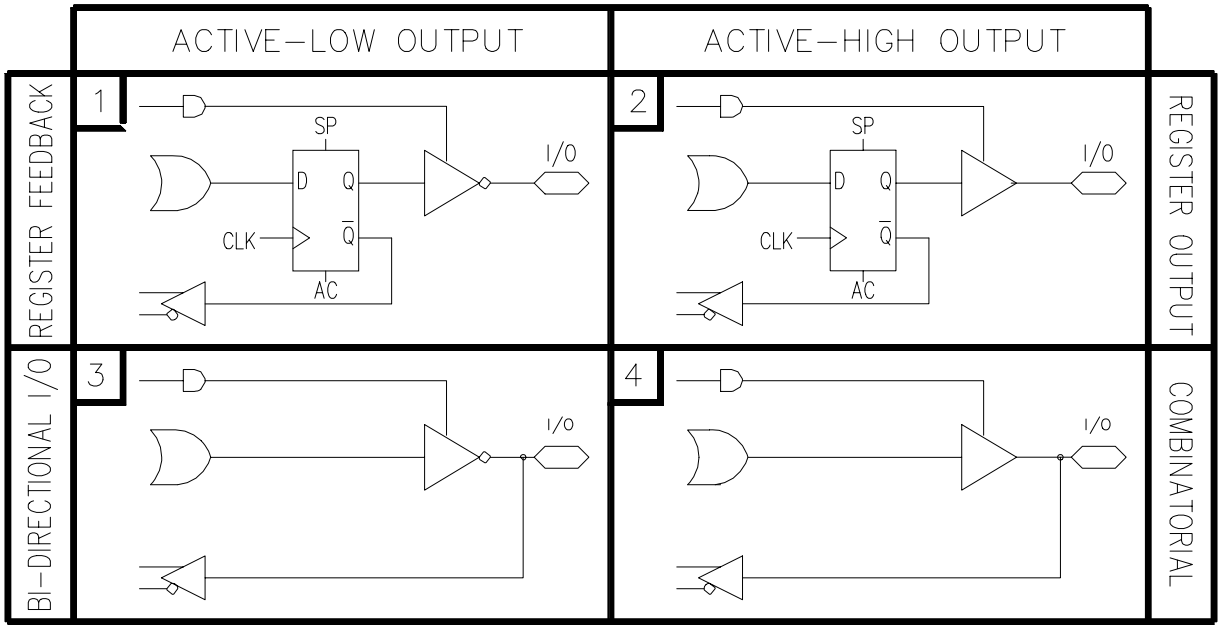


Figure 5. Four Configurations of the PEEL™22CV10A I/O Macrocell

Table 1. PEEL™ 22CV10A Macrocell Configuration Bits

Configuration			Input/Feedback Select	Output Select	
#	A	B			
1	0	0	Register Feedback	Register	Active Low
2	1	0			Active High
3	0	1	Bi-Directional I/O	Combinatorial	Active Low
4	1	1			Active High

Additional Macrocell Configurations

Besides the standard four-configuration macrocells, each PEEL™22CV10A provides an additional eight configurations (twelve total) that can be used to increase design flexibility (see Figure 6 and Table 2). For logic assembly of all twelve configurations, specify PEEL™22CV10A+ and PEEL22CV10A++.

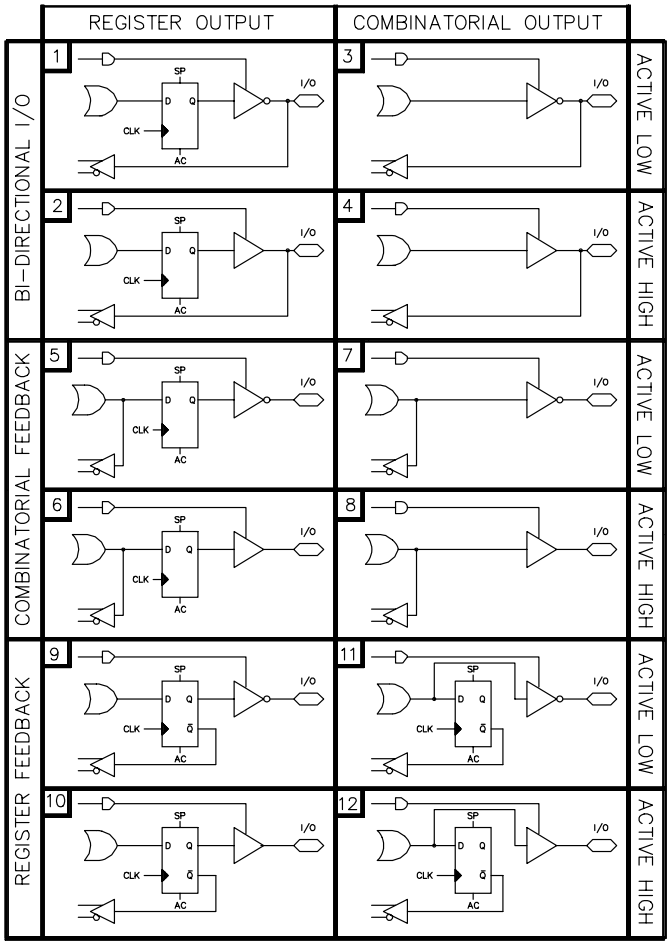


Figure 6. Twelve Configurations of the PEEL™22CV10A+ and PEEL22CV10A++ I/O Macrocell

Table 2. PEEL™ 22CV10A+ & A++ Macrocell Configuration Bits

Configuration		Input/Feedback Select	Output Select	
#	A B C D			
1	1 1 1 1	Bi-Directional I/O	Register	Active Low
2	0 1 1 1			Active High
3	1 0 1 1		Combinatorial	Active Low
4	0 0 1 1			Active High
5	1 1 1 0	Combinatorial Feedback	Register	Active Low
6	0 1 1 0			Active High
7	1 0 1 0		Combinatorial	Active Low
8	0 0 1 0			Active High
9	1 1 0 0	Register Feedback	Register	Active Low
10	1 0 0 0			Active High
11	1 0 0 0		Combinatorial	Active Low
12	0 0 0 0			Active High

Table 6. Absolute Maximum Ratings

This device has been designed and tested for the recommended operating conditions. Improper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Supply Voltage	Relative to Ground	-0.5 to +7.0	V
VI, VO	Voltage Applied to Any Pin[2]	Relative to Ground[1]	-0.5 to VCC+0.6	V
IO	Output Current	Per pin (IOL, IOH)	±25	mA
TST	Storage Temperature		-65 to +150	°C
TLT	Lead Temperature	Soldering 10 second	+300	°C

Table 7. Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
VCC	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	
TA	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
TR	Clock Rise Time	See Note 3		20	ns
TF	Clock Fall Time	See Note 3		20	ns
TRVCC	VCC Rise Time	See Note 3		250	ms

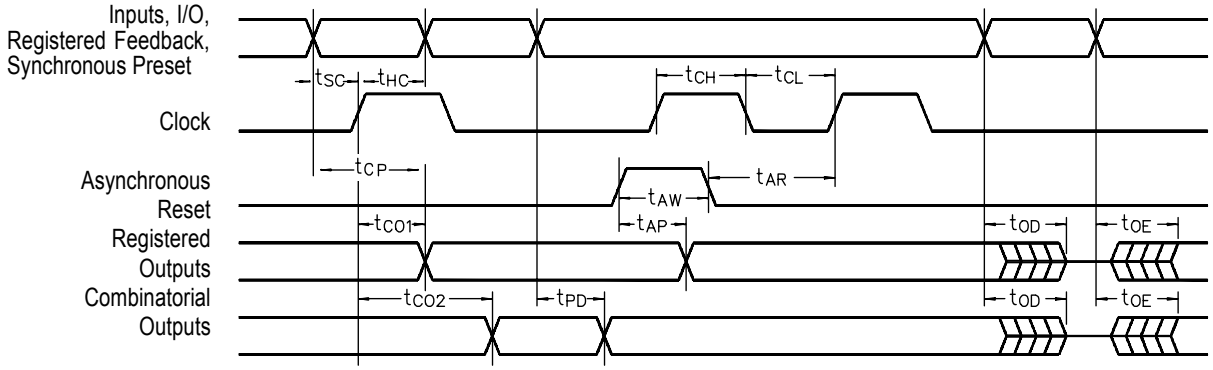
Table 8. D.C. Electrical Characteristics over the recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
VOH	Output HIGH Voltage	VCC=Min, IOH=-4.0mA		2.4		V
VOHC	Output HIGH Voltage-CMOS[13]	VCC=Min, IOH=-10µA		VCC-0.3		V
VOL	Output LOW Voltage-TTL	VCC=Min, IOL=-16mA			0.5	V
VOLC	Output LOW Voltage-CMOS[13]	VCC=Min, IOH=-10µA			0.15	V
VIH	Input HIGH Level			2.0	VCC+0.3	V
VIL	Input LOW Level			-0.3	0.8	V
IIL	Input Leakage Current	VCC=Max, VIN=GND ≤ VIN ≤ VCC			±10	µA
IOZ	Output Leakage Current	I/O=High-Z, GND ≤ VO ≤ VCC			±10	µA
ICC[10]	VCC Current (See CR-1 for typical ICC)	VIN=0V or 3V f=25MHz All outputs diabled[4]	-7/I-7		90/100	mA
			10/I-10		90/100	
			-15/I-15		135/145	
			-25/I-25		30/40	
CIN[7]	Input Capacitance	TA=25°C, VCC=5.0V @f=1MHz			6	pF
COUT[7]	Output Capacitance				12	pF

Table 9. A.C. Electrical Characteristics Over the Operating Range[8,11]

Symbol	Parameter	-1/I-7		-10/I-10		-15/I-15		-25/I-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
tPD	Input[5] to non-registered output		7.5		10		15		25	ns
tOE	Input[5] to output enable[6]		7.5		10		15		25	ns
tOD	Input[5] to output disable[6]		7.5		10		15		25	ns
tCO1	Clock to Output		5.5		6		8		15	ns
tCO2	Clock to comb. output delay via internal registered feedback		10		12		17		35	ns
tCF	Clock to Feedback		3.5		4		5		9	ns
tSC	Input[5] or Feedback Setup to Clock	3		5		8		15		ns
tHC	Input[5] Hold After Clock	0		0		0		0		ns
tCL, tCH	Clock Low Time, Click High Time[8]	3		4		6		13		ns
tCP	Min Clock Period Ext(tSC+tCO1)	8.5		11		18		30		ns
fMAX1	Internal Feedback (1tSC+tCF)[12]	142		111		76.9		41.6		MHz
fMAX2	External Feedback (1/tCP)[12]	117		909		62.5		33.3		MHz
fMAX3	No Feedback (1/tCL+tCH)[12]	166		125		83.3		38.4		MHz
tAW	Asynchronous Reset Pulse Width	7.5		10		15		25		ns
tAP	Input[5] to Asynchronous Reset		7.5		10		15		25	ns
tAR	Asynch. Reset recovery time		7.5		10		15		25	ns
tRESET	Power-on Reset Time for registers in Clear State		5		5		5		5	ns

Switching Waveforms



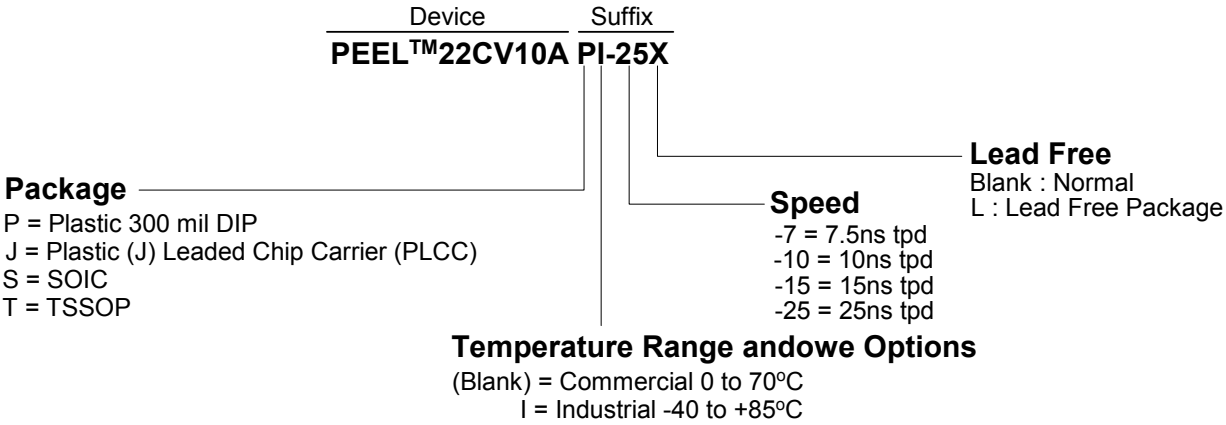
Notes

1. Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
2. V_I and V_O are not specified for program/verify operation.
3. Test points for Clock and V_{CC} in t_R, t_F are referenced at 10% and 90% levels.
4. I/O pins are 0V and 3V.
5. "Input" refers to an Input pin signal.
6. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$, t_{OD} is measured from input transition to V_{OH} -0.1V or V_{OL} +0.1V; $V_{REF} = V_L$ see test loads in Section 5 of the Data Book.
7. Capacitances are tested on a sample basis.
8. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
9. Test one output at a time for a duration of less than 1sec.
10. ICC for a typical application: This parameter is tested with the device programmed as an 8-bit Counter.
11. PEEL™ Device test loads are specified in Section 6 of this Data Book.
12. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design or process modification which may affect operational frequency.
13. Available only for 22CV10A -15/I-15/-25/I-25 grades.

Table 6. Ordering Information

Part Number	Speed	Temperature	Package
PEEL22CV10AP-7 (L)	7.5ns	C	P24
PEEL22CV10API-7 (L)		I	
PEEL 22CV10AJ-7 (L)	7.5ns	C	J28
PEEL 22CV10AJI-7 (L)		I	
PEEL 22CV10AS-7 (L)	7.5ns	C	S24
PEEL 22CV10ASI-7 (L)		I	
PEEL 22CV10AT-7 (L)	7.5ns	C	T24
PEEL 22CV10ATI-7 (L)		I	
PEEL 22CV10AP-10 (L)	10ns	C	P24
PEEL 22CV10API-10 (L)		I	
PEEL 22CV10AJ-10 (L)	10ns	C	J28
PEEL 22CV10AJI-10 (L)		I	
PEEL 22CV10AS-10 (L)	10ns	C	S24
PEEL 22CV10ASI-10 (L)		I	
PEEL 22CV10AT-10 (L)	10ns	C	T24
PEEL 22CV10ATI-10 (L)		I	
PEEL 22CV10AP-15 (L)	15ns	C	P24
PEEL 22CV10API-15 (L)		I	
PEEL 22CV10AJ-15 (L)	15ns	C	J28
PEEL 22CV10AJI-15 (L)		I	
PEEL 22CV10AS-15 (L)	15ns	C	S24
PEEL 22CV10ASI-15 (L)		I	
PEEL 22CV10AT-15 (L)	15ns	C	T24
PEEL 22CV10ATI-15 (L)		I	
PEEL 22CV10AP-25 (L)	25ns	C	P24
PEEL 22CV10API-25 (L)		I	
PEEL 22CV10AT-25 (L)	25ns	C	T24
PEEL 22CV10ATI-25 (L)		I	
PEEL 22CV10AJ-25 (L)	25ns	C	J28
PEEL 22CV10AJI-25 (L)		I	
PEEL 22CV10AS-25 (L)	25ns	C	S24
PEEL 22CV10ASI-25 (L)		I	

Part Number



Anachip Corp.
Head Office ,
2F, No. 24-2, Industry E. Rd. IV, Science-Based
Industrial Park, Hsinchu, 300, Taiwan
Tel: +886-3-5678234
Fax: +886-3-5678368

Anachip USA
780 Montague Expressway, #201
San Jose, CA 95131
Tel: (408) 321-9600
Fax: (408) 321-9696

Email: sales_usa@anachip.com
Website: http://www.anachip.com