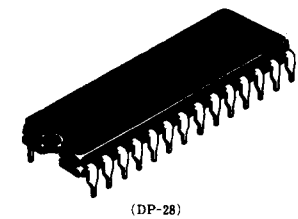
HN61256P, HN61256FP

32768×8-bit or 65536×4-bit CMOS Mask Programmable Read Only Memory

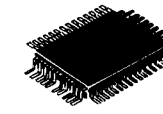
The Hitachi HN61256P/FP is a mask programmable 32768 x 8-bit or 65536x4-bit CMOS read only memory. It operates from a single power supply and is compatible with TTL. Low power consumption makes this memory well-suited for battery-operation or hand-held personal computers. Memory expansion can be implemented through one chip select input. Either active "High" or active "Low" or chip select input and a chip enable input are defined at mask level. The organization of 8 bit or 4 bit is defined by the user.

HN61256P



(DP-28)

HN61256FP

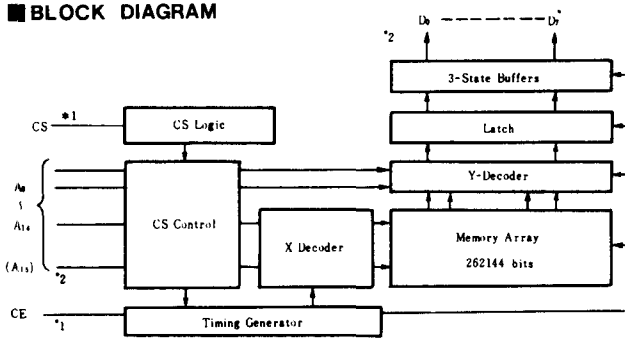


(FP-54)

■FEATURES

- Mask-programmable selection of either 4-bit or 8-bit organization
- Three-state outputs, can be wire-ORed.
- One mask programmable chip select terminal facilitates memory expansion.
- A single 5V power supply (±10%)
- Low power consumption: Operation 7.5mW (typ.), Standby 5μW (typ.)
- TTL compatible
- Access time: 3.5μs (max)

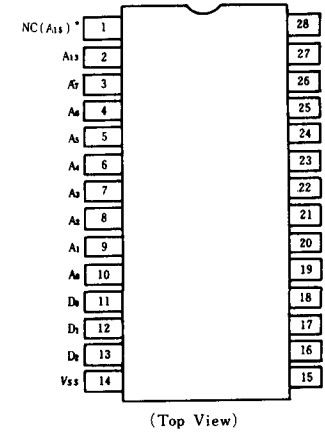
■BLOCK DIAGRAM



*1 Active level defined at mask level.
*2 Mask programmable selection of either 4-bit or 8-bit organization.
In 4-bit organization, data outputs are D0 to D3.

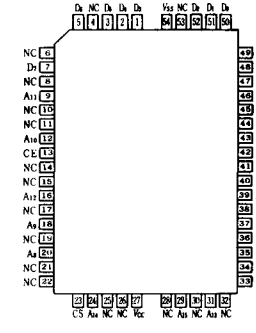
■PIN ARRANGEMENT

●HN61256P



(Top View)

●HN61256FP



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage*	V_{CC}	−0.3～+7.0	V
Input Voltage*	V_{in}	−0.3～+7.0	V
Operating Temperature Range	T_{opr}	0～+75	℃
Storage Temperature Range	T_{stg}	−55～+125	℃
Bias Storage Temperature Range	T_{bias}	−20～+85	℃

Note : * Referenced to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=5V±10%, V_{SS}=0V, Ta=0～+75℃)

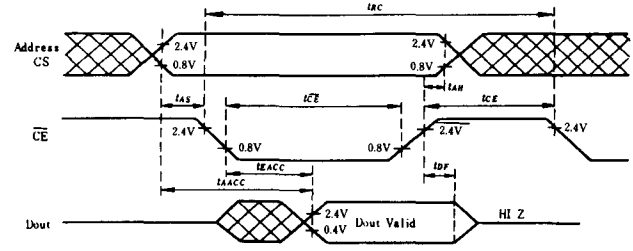
Item		Symbol	Test Condition		min	typ**	max	Unit
Input "High" Level Voltage		V_{IH}			2.4	—	V_{CC}	V
Input "Low" Level Voltage		V_{IL}			0	—	0.8	V
Output "High" Level Voltage		V_{OH}	I_{OH}=−100μA		2.4	—	—	V
Output "Low" Level Voltage		V_{OL}	I_{OL}=1.6mA		—	—	0.4	V
Input Leakage Current		I_{in}	V_{in}=0～5.5V		—	—	2.5	μA
Output "High" Level Leakage Current		I_{LOH}	CE=0.8V	V_{out}=2.4V	—	—	5	μA
Output "Low" Level Leakage Current		I_{LOL}	$\overline{CE}$=2.4V	V_{out}=0.4V	—	—	5	μA
Supply Current	In stand-by	I_{SB}	$\overline{CS}$≧V_{CC}−0.2V, $\overline{CS}$≦V_{SS}+0.2V	V_{CC}=5.5V	—	1	30	μA
	In operation	I_{CC}*	t_{RC}=4.0μs, I_{out}=0mA, $t_{\overline{CE}}$=3.0μs		—	1.5	3.0	mA
Input Capacitance		C_{in}	V_{in}=0V, f=1MHz, Ta=25℃		—	—	10	pF
Output Capacitance		C_{out}			—	—	12.5	pF

* Steady state current ** V_{CC}=5V, T_a=25℃

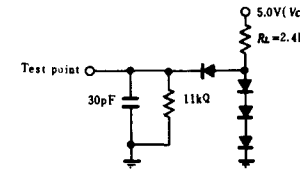
■ AC OPERATING CONDITION AND CHARACTERISTICS

● READ SEQUENCE (V_{CC}=5V±10%, V_{SS}=0V, Ta=0～+75℃, t_r=t_f=20ns)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	4.0	—	μs
Address Access Time	t_{AACC}	—	3.5	μs
Chip Enable Access Time	t_{EACC}	—	3.0	μs
Data Hold Time from Address	t_{DF}	0.05	0.5	μs
Address Set-up Time	t_{AS}	0.5	—	μs
Address Hold Time	t_{AH}	0	—	μs
Chip Enable ON Time	$t_{\overline{CE}}$	3.0	—	μs
Chip Enable OFF Time	t_{CE}	0.5	—	μs



● AC TEST LOAD



Notes : 1. t_r=t_f=20ns.
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

■ ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V±10%, V_{SS} = 0V, T_a = −20 ~ +75 °C)

Item		Symbol	Test Condition		min	typ**	max	Unit
Input Voltage		V_{IH}			2.2	–	V_{CC}	V
		V_{IL}			−0.3	–	0.8	V
Output Voltage		V_{OH}	I_{OH} = −205 μA		2.4	–	–	V
		V_{OL}	I_{OL} = 3.2 mA		–	–	0.4	V
Input Leakage Current		I_{in}	V_{in} = 0 ~ 5.5V		–	–	2.5	μA
Output Leakage Current		I_{LOH}	CS = 0.8V, $\overline{CS}$ = 2.2V	V_{out} = 2.4V	–	–	10	μA
		I_{LOL}		V_{out} = 0.4V	–	–	10	μA
Supply Current	Active	I_{CC}*	V_{CC} = 5.5V, I_{out} = 0mA, t_{RC} = min, duty = 100%.		–	10	30	mA
	Standby	I_{SB}	V_{CC} = 5.5V, $\overline{CS}$ ≧ V_{CC} − 0.2V, CS ≦ 0.2V		–	1	30	μA
Input Capacitance		C_{in}	V_{in} = 0V, f = 1 MHz, T_a = 25 °C		–	–	10	pF
Output Capacitance		C_{out}			–	–	15	pF

* Steady state current
** V_{CC}=5V, T_a=25°C

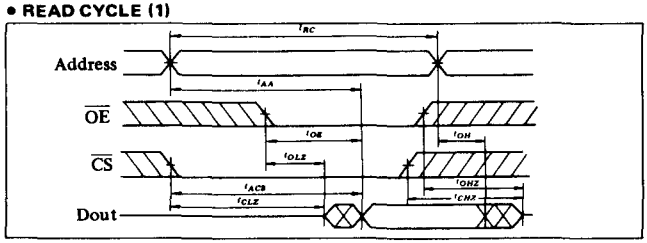
■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

(V_{CC}=5V±10%, V_{SS}=0V, Ta=−20~+75°C, t_r=t_f=20ns)

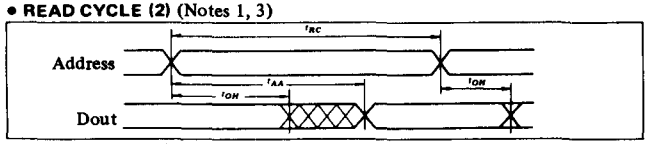
Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	200	–	ns
Address Access Time	t_{AA}	–	200	ns
Chip Select Access Time	t_{ACS}	–	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	ns
Output Enable to Output Valid	t_{OE}	–	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	100	ns
Chip Disable to Output in High Z	t_{OHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	–	ns

■ TIMING WAVEFORM

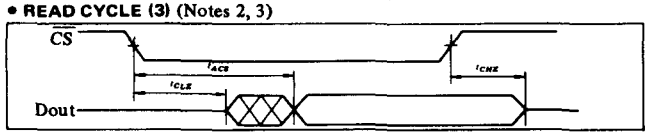
• READ CYCLE (1)



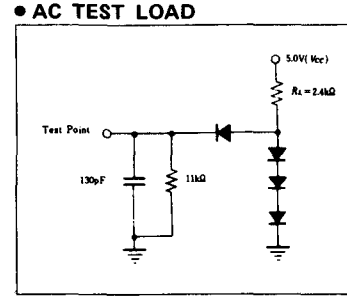
• READ CYCLE (2) (Notes 1, 3)



• READ CYCLE (3) (Notes 2, 3)



• AC TEST LOAD



Notes : 1. t_r = t_f = 20ns
2. C_L includes jig capacitance
3. All diodes are 1S2074Ⓗ

NOTES:

1. Device is continuously selected.
2. Address Valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{OE}$ = V_{IL}.
4. Input pulse level: 0.8 to 2.4V
5. Input and output reference level: 1.5V