# HN58C66 Series

8192-word × 8-bit CMOS Electrically Erasable and Programmable CMOS ROM

HITACHI

ADE-203-375F (Z)
Rev. 6.0
Apr. 12, 1995

## Description

The Hitachi HN58C66 is a electrically erasable and programmable ROM organized as 8192-word × 8-bit. It realizes high speed, low power consumption, and a high level of reliability, employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 32-byte page programming function to make its erase and write operations faster.

## Features

- Single 5 V supply
- On chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (32 bytes): 10 ms max
- High speed: Access time 250 ns max
- Low power dissipation:
  20 mW/MHz typ (active)
  2.0 mW typ (standby)
- $\overline{Data}$ polling, RDY/$\overline{Busy}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- $10^5$ erase/write cycles (in page mode)
- 10 years data retension
- Write protection by $\overline{RES}$ pin

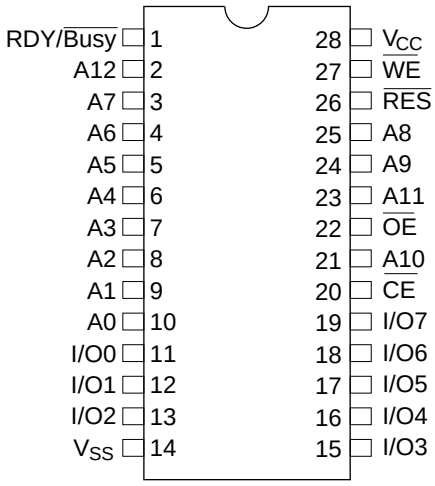
## Ordering Information

| Type No | Access Time | Package |
|---|---|---|
| HN58C66P-25 | 250 ns | 600-mil 28-pin plastic DIP (DP-28) |
| HN58C66FP-25 | 250 ns | 28-pin plastic SOP[*1] (FP-28D/DA) |
| HN58C66T-25 | 250 ns | 32-pin plastic TSOP (TFP-32DA) |

Note: 1. T is added to the end of the type no. for a SOP of 3.00 mm (max) thickness.

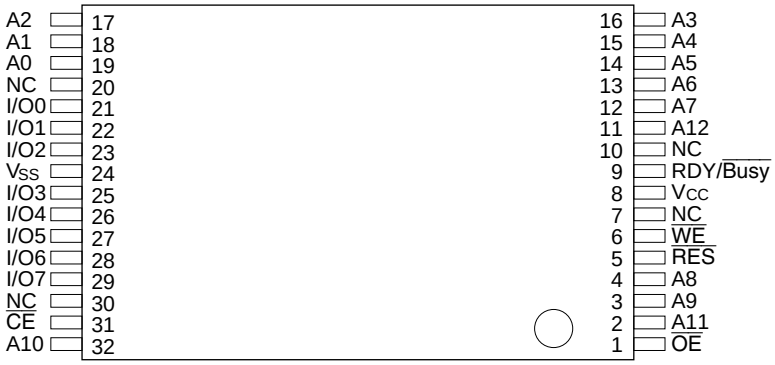
## Pin Arrangement

HN58C66P/FP Series




(Top View)

HN58C66T Series

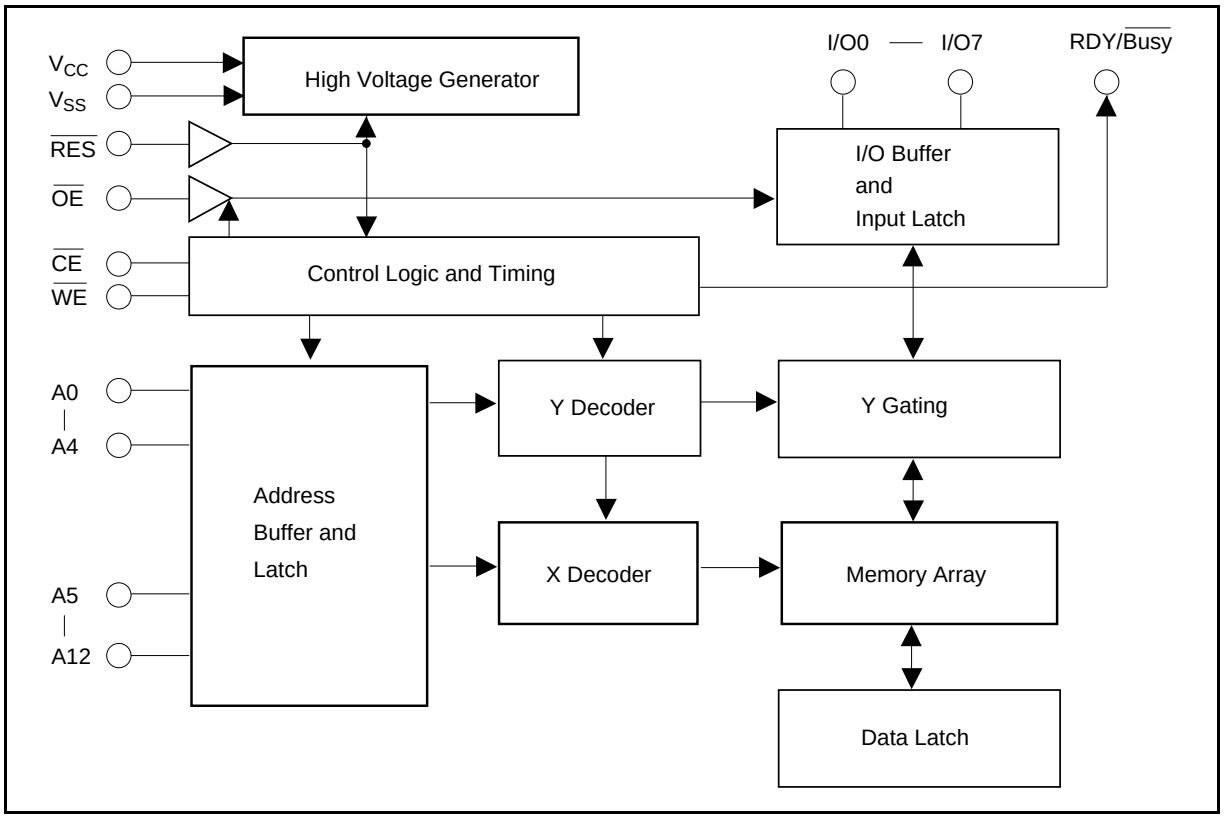



(Top View)

## Pin Description

| Pin Name | Function |
|---|---|
| A0 – A12 | Address |
| I/O0 – I/O7 | Data input/output |
| $\overline{OE}$ | Output enable |
| $\overline{CE}$ | Chip enable |
| $\overline{WE}$ | Write enable |
| $V_{CC}$ | Power supply (+5 V) |
| $V_{SS}$ | Ground |
| $\overline{RES}$ | Reset |
| NC | No connection |
| RDY/$\overline{Busy}$ | Ready/$\overline{Busy}$ |

## Block Diagram



## Mode Selection

| Pin Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | RDY/$\overline{Busy}$ | $\overline{RES}$ | I/O |
|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | High-Z | $V_H$ [*1] | Dout |
| Standby | $V_{IH}$ | X [*2] | X | High-Z | X | High-Z |
| Write | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | High-Z to $V_{OL}$ | $V_H$ | Din |
| Deselect | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | High-Z | $V_H$ | High-Z |
| Write inhibit | X | X | $V_{IH}$ | High-Z | X | — |
| | X | $V_{IL}$ | X | | | |
| $\overline{Data}$ polling | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{OL}$ | $V_H$ | Data out (I/O7) |
| Program reset | X | X | X | High-Z | $V_{IL}$ | High-Z |

Notes: 1. Refer to the recommended DC operating condition.
2. X = Don't care.

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage [*1] | $V_{CC}$ | –0.6 to +7.0 | V |
| Input voltage [*1] | Vin | –0.5 [*2] to +7.0 | V |
| Operating temperature range [*3] | Topr | 0 to +70 | °C |
| Storage temperature range | Tstg | –55 to +125 | °C |

Notes: 1. With respect to $V_{SS}$
2. Vin min = –3.0 V for pulse width ≤ 50 ns
3. Including electrical characteristics and data retention

## Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input voltage | $V_{IL}$ | –0.3 | — | 0.8 | V |
| | $V_{IH}$ | 2.2 | — | $V_{CC}$ + 1.0 | V |
| | $V_H$ | $V_{CC}$ – 0.5 | — | $V_{CC}$ + 1.0 | V |
| Operating temperature | Topr | 0 | — | 70 | °C |

## DC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ± 10%)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | — | — | 2[*1] | µA | $V_{CC}$ = 5.5 V, Vin = 5.5 V |
| Output leakage current | $I_{LO}$ | — | — | 2 | µA | $V_{CC}$ = 5.5 V, Vout = 5.5/0.4 V |
| $V_{CC}$ current (standby) | $I_{CC1}$ | — | — | 1 | mA | $\overline{CE}$ = $V_{IH}$, $\overline{CE}$ = $V_{CC}$ |
| $V_{CC}$ current (active) | $I_{CC2}$ | — | — | 8 | mA | Iout = 0 mA, Duty = 100%, Cycle = 1 µs at $V_{CC}$ = 5.5 V |
| | | — | — | 25 | mA | Iout = 0 mA, Duty = 100% Cycle = 250 ns at $V_{CC}$ = 5.5 V |
| Input low voltage | $V_{IL}$ | –0.3[*2] | — | 0.8 | V | |
| Input high voltage | $V_{IH}$ | 2.2 | — | $V_{CC}$ + 1.0 | V | |
| | $V_H$ | $V_{CC}$ – 0.5 | — | $V_{CC}$ + 1.0 | V | |
| Output low voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 2.1 mA |
| Output high voltage | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = –400 µA |

Notes: 1. $I_{LI}$ on $\overline{RES}$ = 100 µA max.
2. $V_{IL}$ min = –1.0 V for pulse width ≤ 50 ns

## Capacitance (Ta = 25°C, f = 1 MHz)

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input capacitance | Cin[*1] | — | — | 6 | pF | Vin = 0 V |
| Output capacitance | Cout[*1] | — | — | 12 | pF | Vout = 0 V |

Note: 1. This parameter is periodically sampled and not 100% tested.

## AC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ± 10%)

### Test Conditions

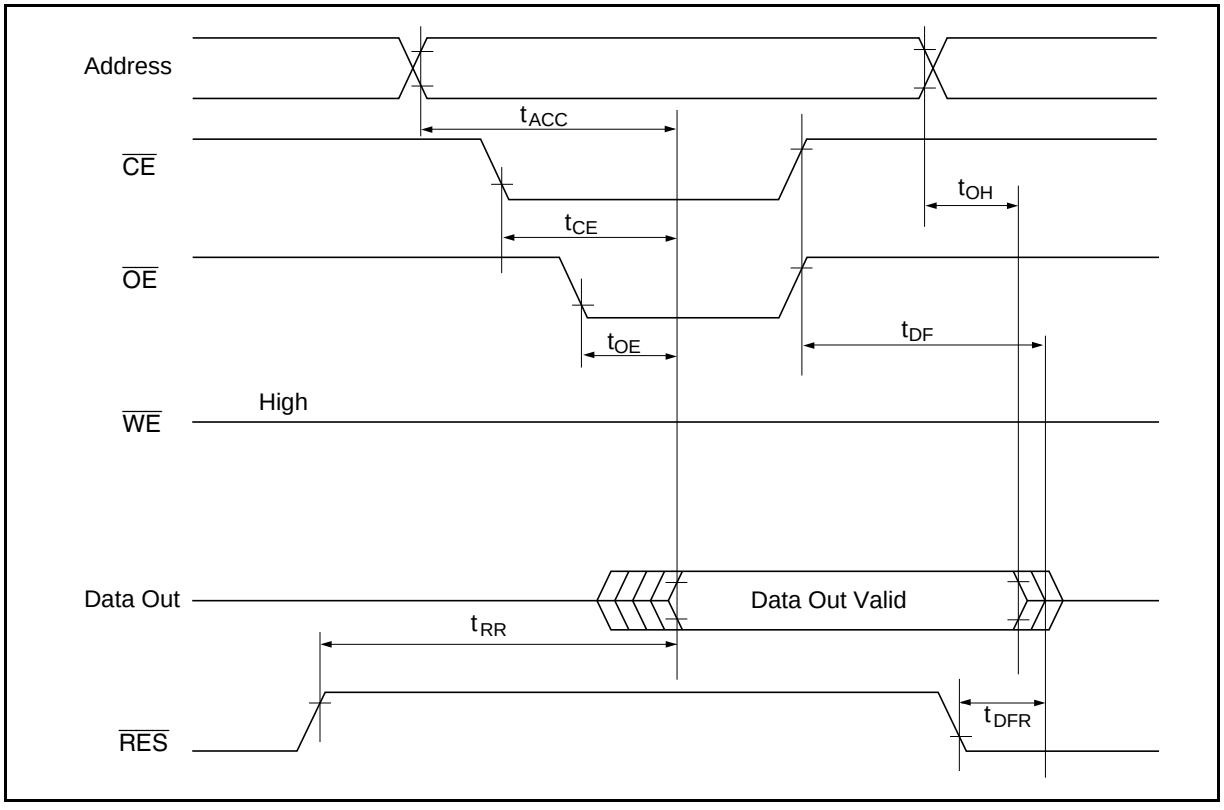
- Input pulse levels: 0.4 V to 2.4 V, 0 to $V_{CC}$ ($\overline{RES}$ pin)
- Input rise and fall time: ≤ 20 ns
- Output load: 1TTL gate +100 pF
- Reference levels for measuring timing: 0.8 V, 2.0 V

### Read Cycle

| Parameter | Symbol | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| Address to output delay | $t_{ACC}$ | — | 250 | ns | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$ |
| $\overline{CE}$ to output delay | $t_{CE}$ | — | 250 | ns | $\overline{OE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$ |
| $\overline{OE}$ to output delay | $t_{OE}$ | 10 | 100 | ns | $\overline{CE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$ |
| $\overline{OE}$ ($\overline{CE}$) high to output float*1 | $t_{DF}$ | 0 | 90 | ns | $\overline{CE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$ |
| $\overline{RES}$ low to output float*1 | $t_{DFR}$ | 0 | 350 | ns | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$ |
| Data output hold | $t_{OH}$ | 0 | — | ns | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$ |
| $\overline{RES}$ to output delay | $t_{RR}$ | 0 | 450 | ns | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$ |

Note: 1. $t_{DF}$, $t_{DFR}$ is defined at which the outputs achieve the open circuit conditions and are no longer driven.

### Read Timing Waveform



### Write Cycle

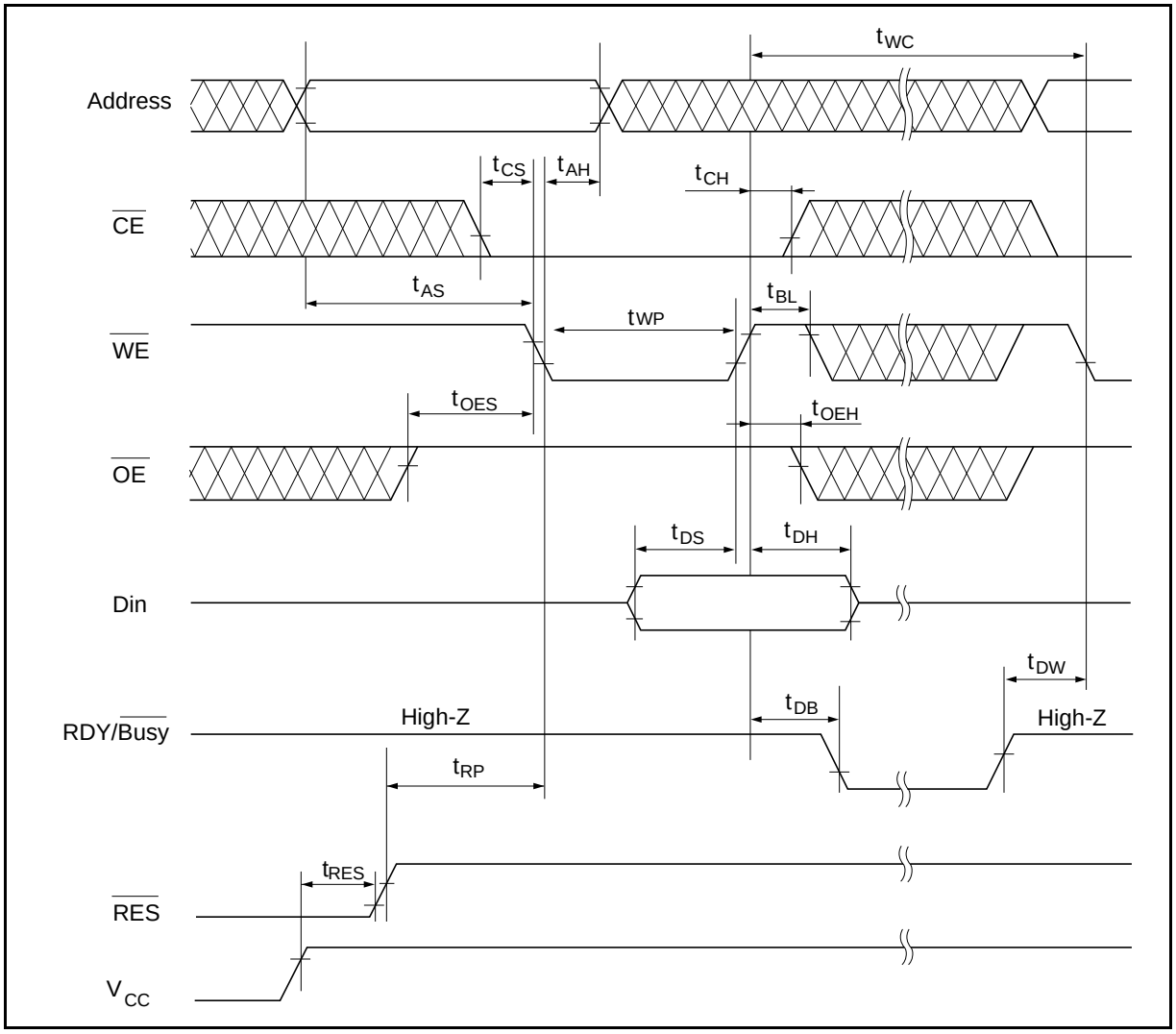
| Parameter | Symbol | Min[*1] | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Address setup time | $t_{AS}$ | 0 | — | — | ns | |
| Address hold time | $t_{AH}$ | 150 | — | — | ns | |
| $\overline{CE}$ to write setup time ($\overline{WE}$ controlled) | $t_{CH}$ | 0 | — | — | ns | |
| $\overline{CE}$ hold time ($\overline{WE}$ controlled) | $t_{CH}$ | 0 | — | — | ns | |
| $\overline{WE}$ to write setup time ($\overline{CE}$ controlled) | $t_{WS}$ | 0 | — | — | ns | |
| $\overline{WE}$ hold time ($\overline{CE}$ controlled) | $t_{WH}$ | 0 | — | — | ns | |
| $\overline{OE}$ to write setup time | $t_{OES}$ | 0 | — | — | ns | |
| $\overline{OE}$ hold time | $t_{OEH}$ | 0 | — | — | ns | |
| Data setup time | $t_{DS}$ | 100 | — | — | ns | |
| Data hold time | $t_{DH}$ | 20 | — | — | ns | |
| $\overline{WE}$ pulse width ($\overline{WE}$ controlled) | $t_{WP}$ | 200 | — | — | ns | |
| $\overline{CE}$ pulse width ($\overline{CE}$ controlled) | $t_{CW}$ | 200 | — | — | ns | |
| Data latch time | $t_{DL}$ | 100 | — | — | ns | |
| Byte load cycle | $t_{BLC}$ | 0.30 | — | 30 | µs | |
| Byte load window | $t_{BL}$ | 100 | — | — | µs | |
| Write cycle time | $t_{WC}$ | — | — | 10[*2] | ms | |
| Time to device busy | $t_{DB}$ | 120 | — | — | ns | |
| Write start time | $t_{DW}$ | 150[*3] | — | — | ns | |
| Reset protect time | $t_{RP}$ | 100 | — | — | µs | |
| Reset high time | $t_{RES}$ | 1 | — | — | µs | |

Notes: 1. Use this device in longer cycle than this value.

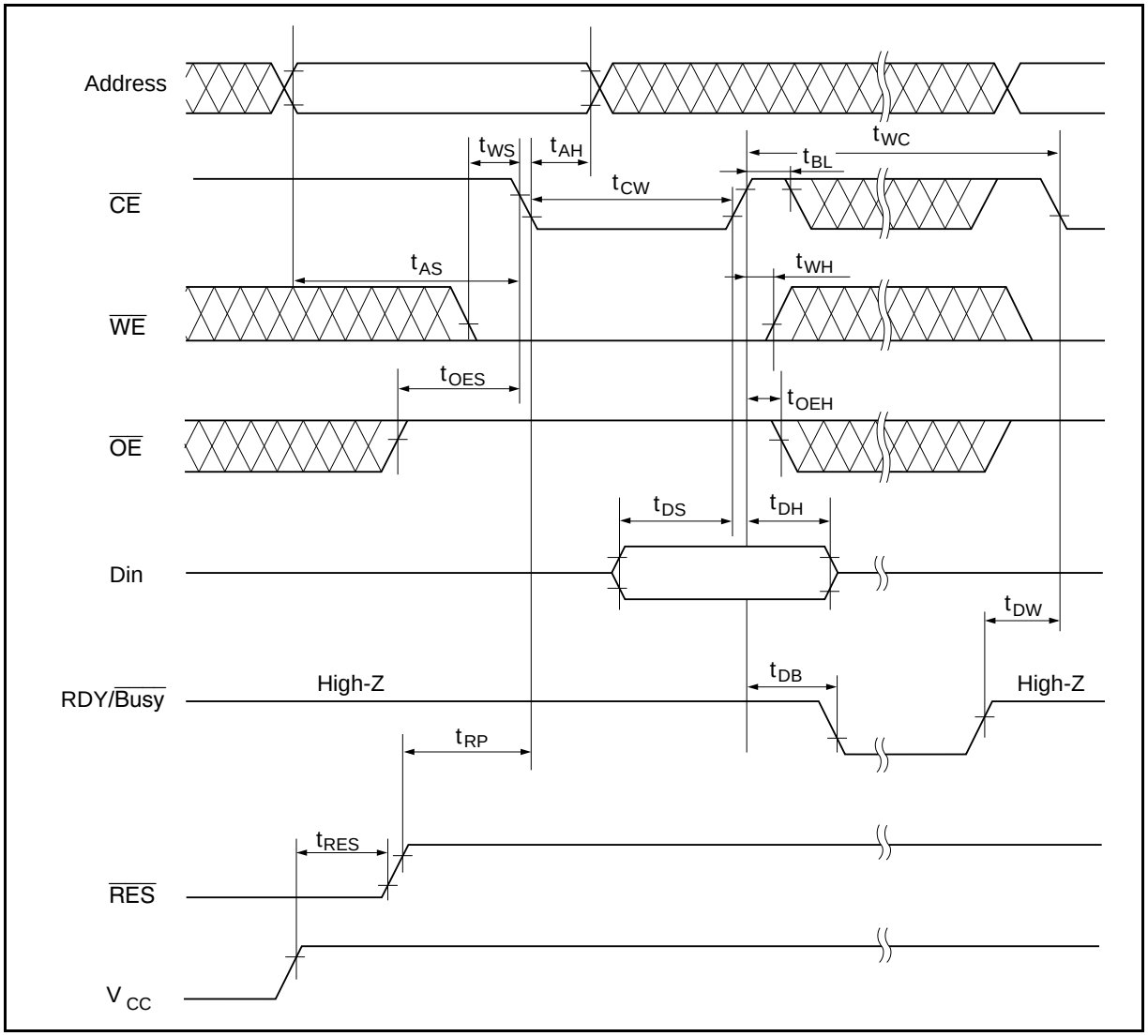
2. $t_{WC}$ must be longer than this value unless polling technique or RDY/$\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.

3. Next read or write operation can be initiated after $t_{DW}$ if polling technique or RDY/$\overline{Busy}$ are used.

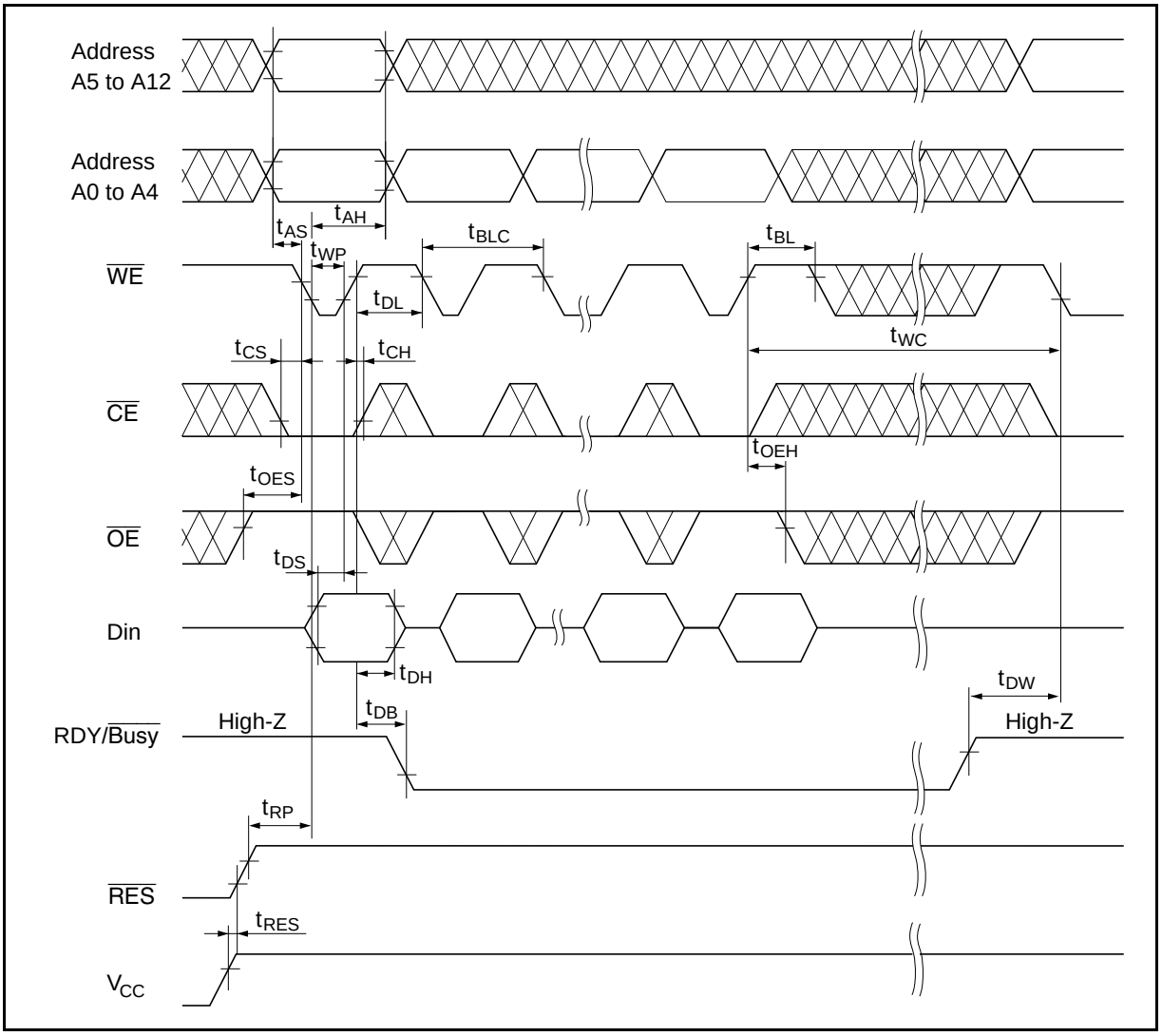
**Byte Write Timing Waveform (1)** ($\overline{WE}$ Controlled)



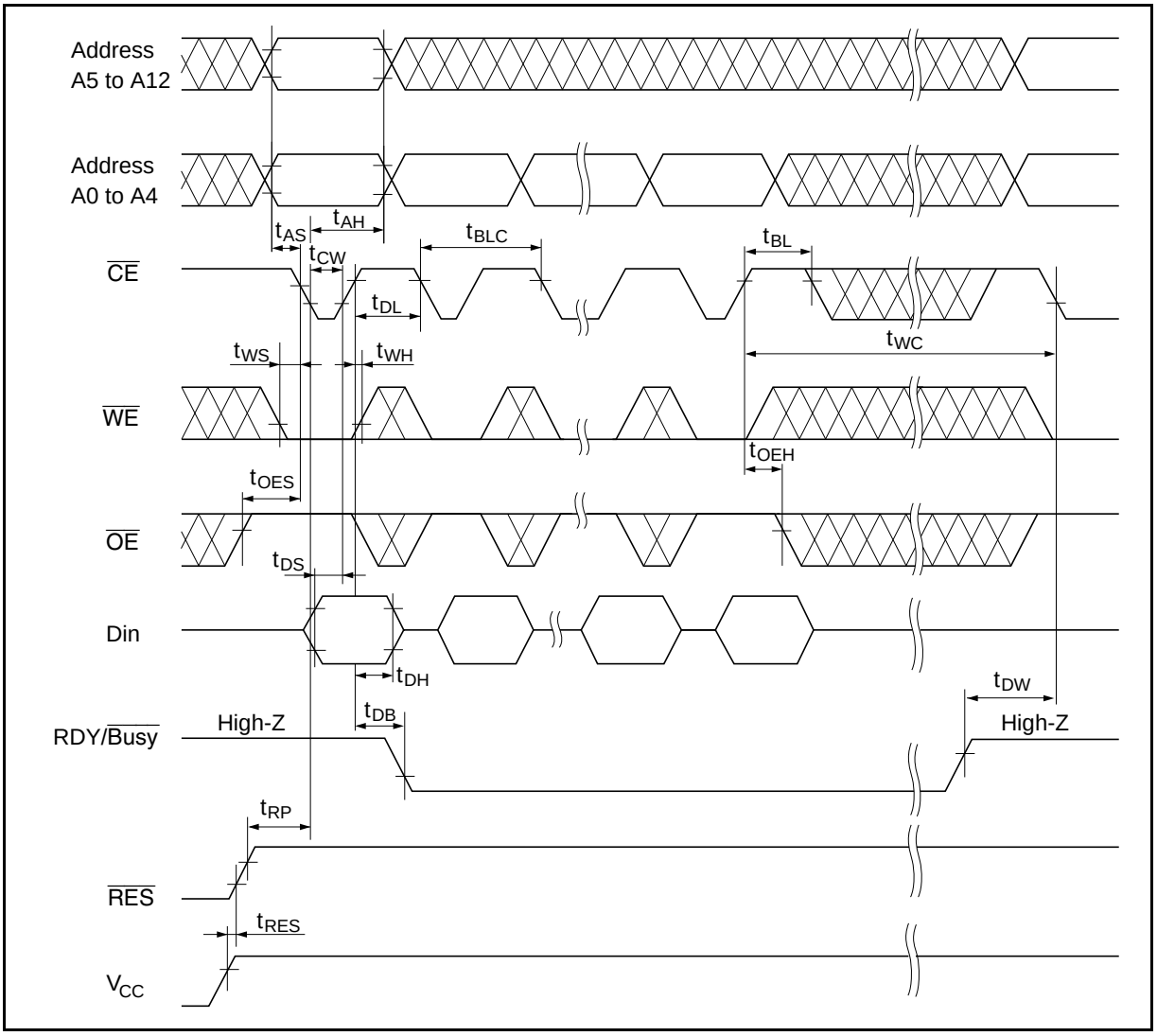
**Byte Write Timing Waveform (2)** ($\overline{CE}$ Controlled)



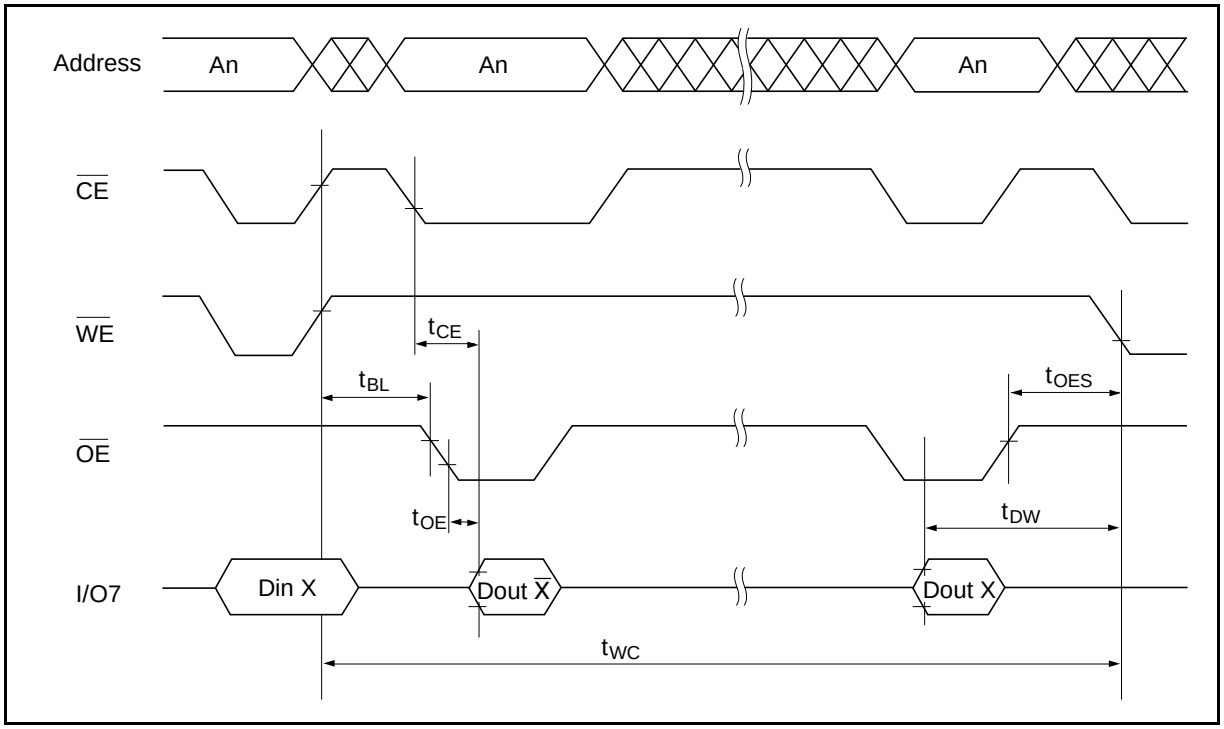
**Page Write Timing Waveform (1)** ($\overline{WE}$ Controlled)



**Page Write Timing Waveform (2)** ($\overline{CE}$ Controlled)



**$\overline{\text{Data}}$ Polling Timing Waveform**



## Functional Description

### Automatic Page Write

Page-mode write feature allows 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 31 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ or $\overline{WE}$ is high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

### $\overline{\text{Data}}$ Polling

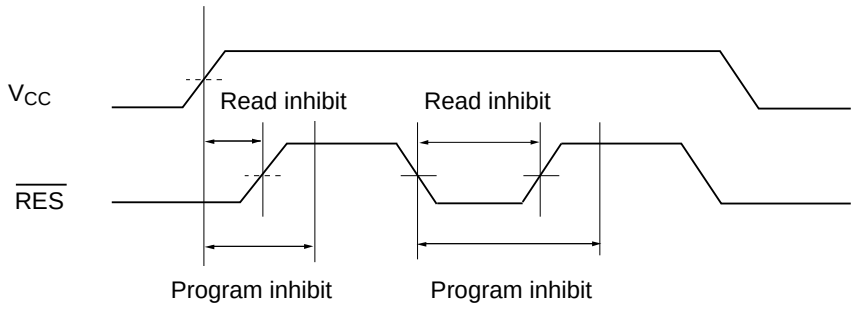
$\overline{\text{Data}}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

**RDY/$\overline{\text{Busy}}$ Signal**

RDY/$\overline{\text{Busy}}$ signal also allows the status of the EEPROM to be determined. The RDY/$\overline{\text{Busy}}$ signal has high impedance except in write cycle and is lowered to $V_{OL}$ after the first write signal. At the end of a write cycle, the RDY/$\overline{\text{Busy}}$ signal changes state to high impedance.

**$\overline{\text{RES}}$ Signal**

When $\overline{\text{RES}}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{\text{RES}}$ low when $V_{CC}$ is switched. $\overline{\text{RES}}$ should be high during read and programming because it doesn't provide a latch function.




**$\overline{\text{WE}}$, $\overline{\text{CE}}$ Pin Operation**

During a write cycle, addresses are latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, and data is latched by the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$.

**Write/Erase Endurance and Data Retention**

The endurance is $10^5$ cycles in case of the page programming and $3 \times 10^3$ cycles in case of byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than $10^4$ cycles.

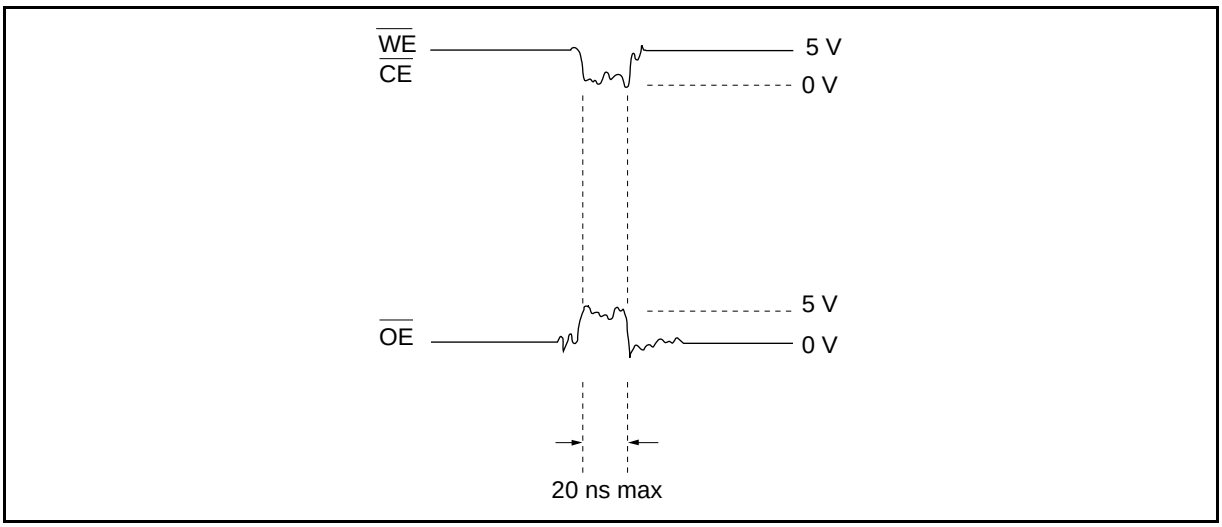
**Data Protection**

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to program mode by mistake.

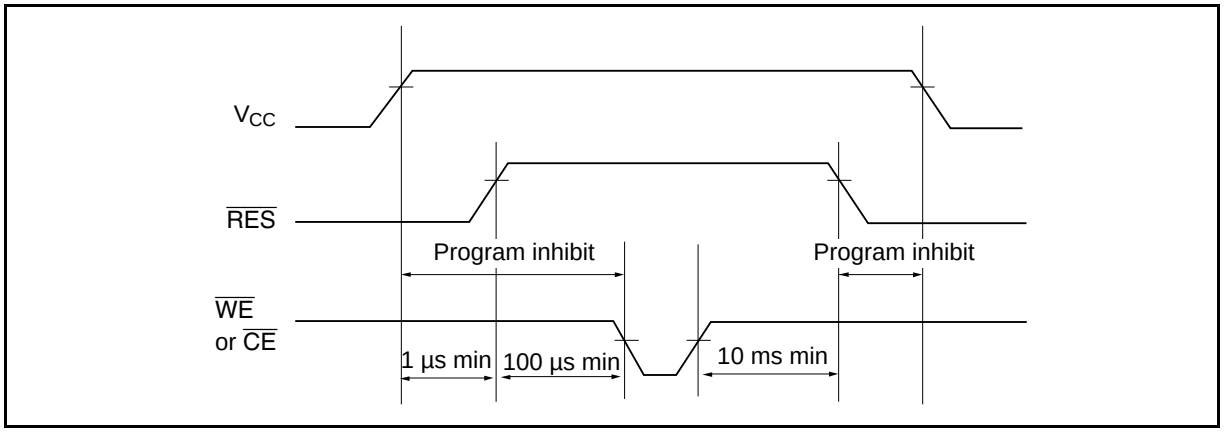
   To prevent this phenomenon, this device has a noise cancelation function that cuts noise if its width is 20 ns or less in program mode.

   Be careful not to allow noise of a width of more than 20 ns on the control pins.



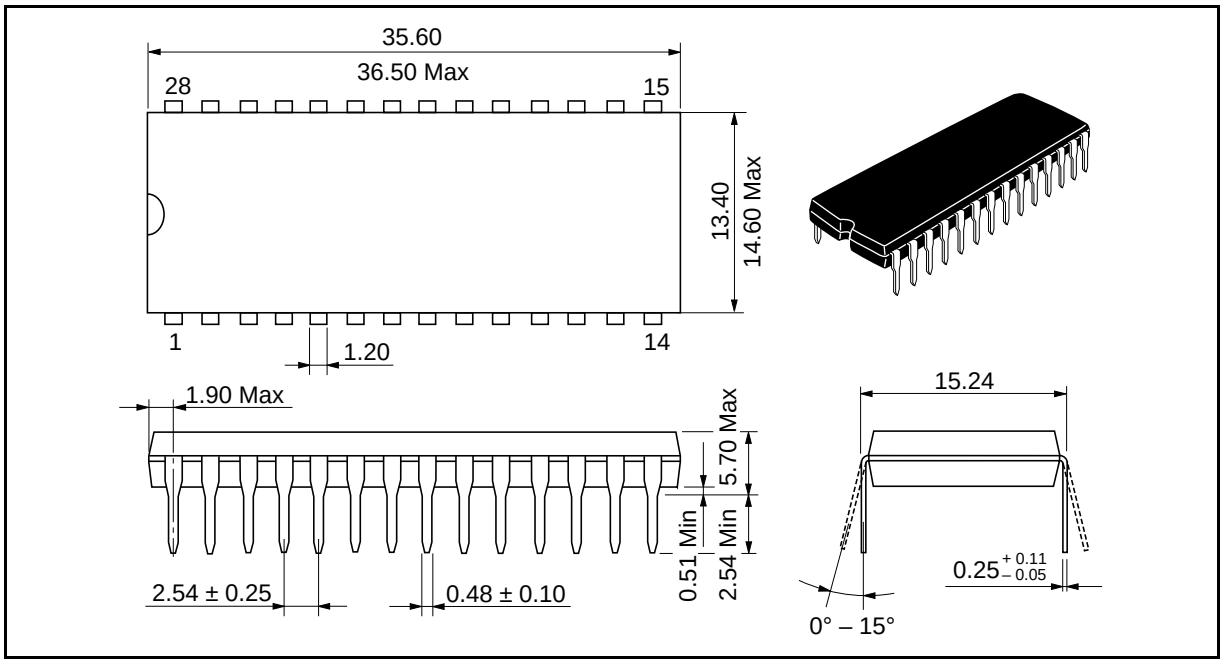
2. Data Protection at $V_{CC}$ On/Off

When $V_{CC}$ is turned on or off, the noise on the control pins generated by external circuits (CPU, etc.) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state by using a CPU reset signal to $\overline{RES}$ pin. $\overline{RES}$ pin should be kept at $V_{SS}$ level when $V_{CC}$ is turned on and off. The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.

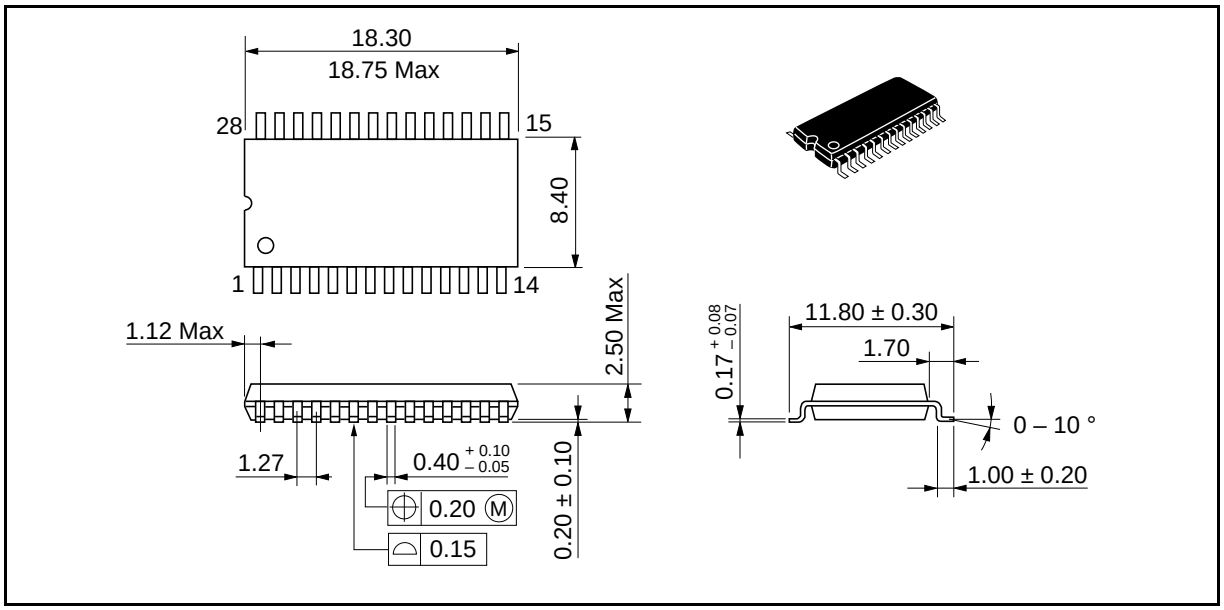


## Package Dimensions

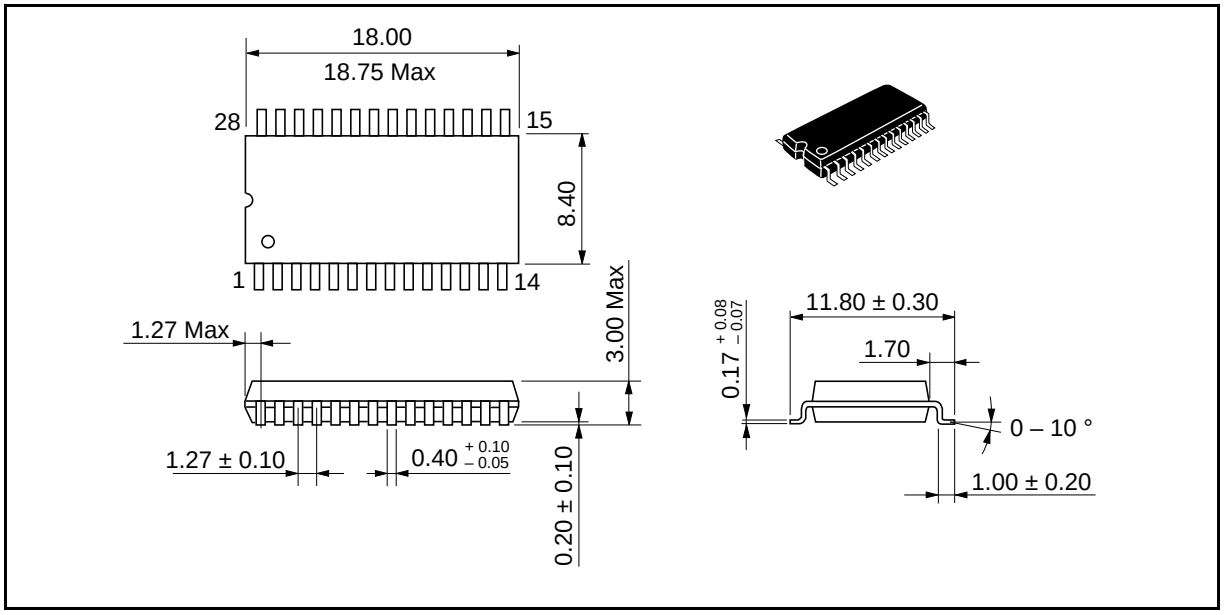
**HN58C66P Series** (DP-28) Unit: mm




**HN58C66FP Series** (FP-28D) Unit: mm



**HN58C66FP Series** (FP-28DA) Unit: mm




**HN58C66T Series** (TFP-32DA) Unit: mm