

700 Bit Serial Electrically Alterable Read Only Memory

FEATURES

- 50 word x 14 bit organization
- Addressing by two consecutive one-of-ten codes
- Word alterable
- 10 year data storage
- TTL compatible signal levels
- Write/erase time: 10ms

DESCRIPTION

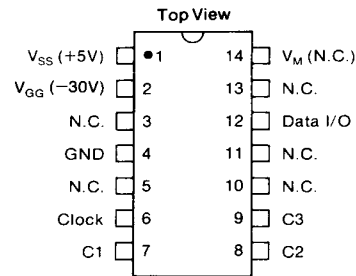
The ER1451 is a serial input/output 700 bit electrically erasable and reprogrammable ROM, organized as 50 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus. Its operation is similar to the ER1400 in all respects, except that it has only half the memory capacity. The address, in the form of two consecutive one-of-ten codes, is shifted in with the first ten bits indicating the MSD. Address 49 is the highest valid address. For this reason during the first five clock cycles of an ACCEPT ADDRESS function the data input is ignored.

Mode selection is by a 3 bit code applied to C1, C2 and C3.

Before writing, a selected location must be preconditioned by an Erase operation. Data is then stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 700 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

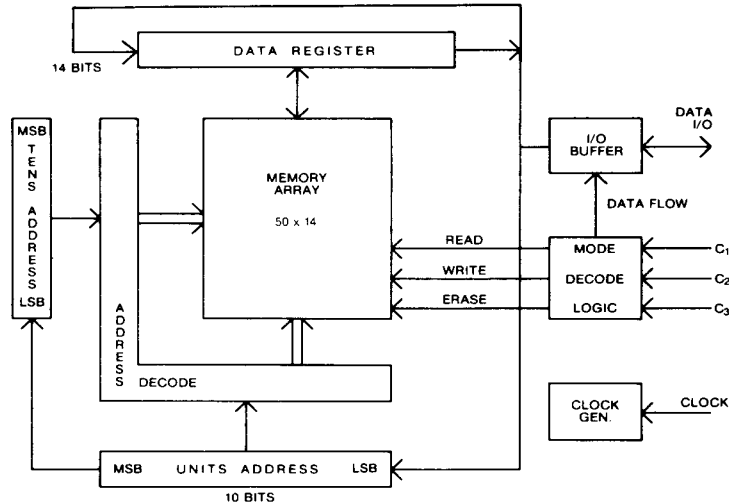
ELEC. ALTERABLE
NON-VOLATILE MEMORY

PIN CONFIGURATION 14 LEAD DUAL IN LINE



N.C. = No external connection
for normal usage

BLOCK DIAGRAM



PIN FUNCTIONS

Name	Function																																				
Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respectively. When outputting data it has TTL drive capability, while in all other modes it is left floating.																																				
V _M	Used for testing purposes only. Must be left unconnected for normal operation.																																				
V _{SS}	Chip substrate. Normally connected to +5V																																				
V _{GG}	DC supply. Normally connected to -30 Volt supply.																																				
Clock	Timing reference. Required for all operations. May be left at logic one when device is in standby.																																				
C1, C2, C3	Mode control pins. Their operation is as follows:																																				
	<table border="1"> <thead> <tr> <th>C1</th> <th>C2</th> <th>C3</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Standby—The output buffer is left floating. If the clock is maintained, the contents of the Address and Data Registers will remain unchanged.</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Accept Address—Data presented at the I/O pin is shifted into the Address Register with each clock pulse. Addressing is by two consecutive one-of-ten codes.</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Read—The address word is read from memory into the data register.</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Shift Data Out—The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Erase—The word stored at the addressed location is erased to all zeroes.</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Accept Data—The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Write—The word contained in the Data Register is written into the location designated by the Address Register.</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Not Used</td> </tr> </tbody> </table>	C1	C2	C3	Function	1	1	1	Standby—The output buffer is left floating. If the clock is maintained, the contents of the Address and Data Registers will remain unchanged.	1	0	0	Accept Address—Data presented at the I/O pin is shifted into the Address Register with each clock pulse. Addressing is by two consecutive one-of-ten codes.	0	1	1	Read—The address word is read from memory into the data register.	0	1	0	Shift Data Out—The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.	1	0	1	Erase—The word stored at the addressed location is erased to all zeroes.	0	0	0	Accept Data—The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.	0	0	1	Write—The word contained in the Data Register is written into the location designated by the Address Register.	1	1	0	Not Used
C1	C2	C3	Function																																		
1	1	1	Standby—The output buffer is left floating. If the clock is maintained, the contents of the Address and Data Registers will remain unchanged.																																		
1	0	0	Accept Address—Data presented at the I/O pin is shifted into the Address Register with each clock pulse. Addressing is by two consecutive one-of-ten codes.																																		
0	1	1	Read—The address word is read from memory into the data register.																																		
0	1	0	Shift Data Out—The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.																																		
1	0	1	Erase—The word stored at the addressed location is erased to all zeroes.																																		
0	0	0	Accept Data—The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.																																		
0	0	1	Write—The word contained in the Data Register is written into the location designated by the Address Register.																																		
1	1	0	Not Used																																		

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (except V _{GG}) with respect to V _{SS} . . . -20V to +0.3V
V _{GG} with respect to V _{SS} -40V
Storage temperature (No Data Retention) -65°C to +150°C
Storage temperature (with Data Retention)
Operating -25°C to +75°C
Unpowered -65°C to +80°C

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted)

V _{SS} = +5 Volts ± 5% GND = 0 Volts
V _{GG} = -30 Volts ± 5%
Operating Temperature T _A = 0°C to +70°C

Characteristics	Sym	Min	Typ**	Max	Units	Conditions	
DC CHARACTERISTICS							
Input Logic "0"	V _{IL}	V _{SS} -15.0	—	+0.8	Volts	V _{IN} = -10V I _{OL} = 3.2mA I _{OH} = 3.2mA	
Input Logic "1"	V _{IH}	V _{SS} -1.5	—	V _{SS} +0.3	Volts		
Input Leakage	I _L	—	—	10	μA		
Output Logic "0"	V _{OL}	—	—	+0.4	Volts		
Output Logic "1"	V _{OH}	V _{SS} -1.5	—	V _{SS}	Volts		
Power Consumption	P _{GG}	—	—	300	mW		
Power Supply Current	I _{GG}	—	—	8.0	mA		
	I _{SS}	—	—	8.0	mA		
AC CHARACTERISTICS							
Clock Frequency	f _φ	10.0	14.0	17.0	kHz		
Clock Duty Cycle	D _φ	35	50	65	%		
Write Time	t _w	10.0	15.0	24.0	ms		
Erase Time	t _e	10.0	15.0	24.0	ms		
Rise, Fall Time	t _r , t _f	—	—	1.0	μs		
Control, Data Set Up Time	t _{CS}	1	—	—	μs		
Control, Data Hold Time	t _{CH}	0	—	—	μs		
Propagation Delay	t _{pw}	—	—	20.0	μs	Load: 2 TTL gates + 100pF	
Non-Volatile Data Storage	T _S	10	—	—	Years	See Note 1.	
Number of Erase/Write Cycles	N _w	—	—	10 ⁴	—	Per word. See Note 2.	
Number of Read Accesses Between Writes	N _{RA}	10 ⁹	—	—	—	Per word	

** Typical values are at +25°C and nominal voltages.

NOTES: 1. T_S is for powered or unpowered storage.

2. N_w (=10⁴) is a maximum for data retention times greater than 10 years. Beyond 10⁴ reprogramming cycles, there is a gradual, logarithmic reduction in retention time with 1 year being a typical value after 10⁵ cycles.

ELEC. ALTERABLE
NON-VOLATILE MEMORY

ELEC. ALTERABLE
NON-VOLATILE MEMORY

TIMING DIAGRAMS

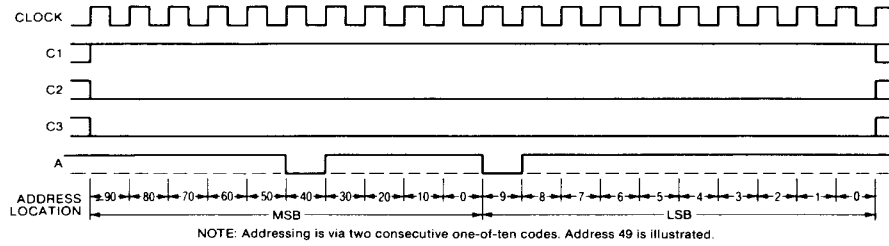


Fig.1 ACCEPT ADDRESS

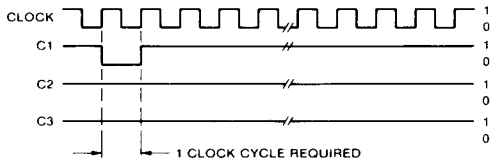
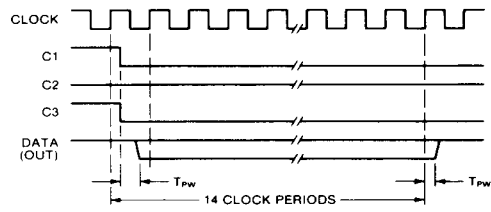


Fig.2 READ



T_{pw} measured initially from control line transition to data out then measured from the positive clock edges to data changes. Timing measurements made at $V_{SS} - 2$ and 0.8 Volt points.

Fig.3 SHIFT DATA OUT

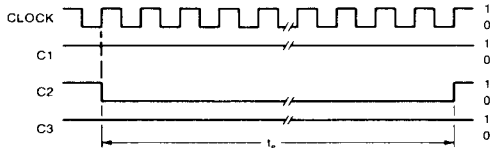


Fig.4 ERASE

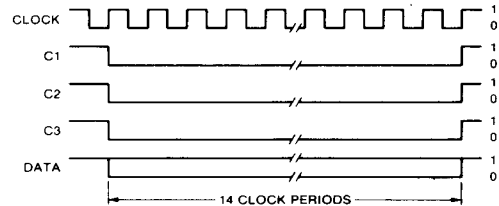


Fig.5 ACCEPT DATA

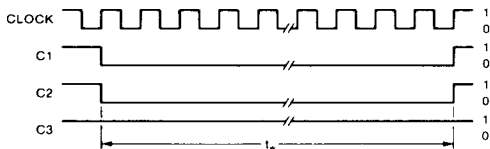


Fig.6 WRITE

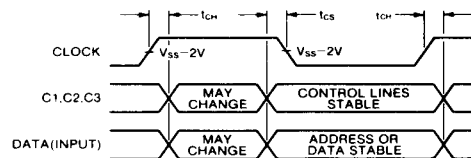


Fig.7 INPUT TIMING