Features

- **Fast Read Access Time - 120 ns**
- **Dual Voltage Range Operation**
  - **Unregulated Battery Power Supply Range, 2.7V to 3.6V or Standard 5V ± 10% Supply Range**
- **Pin Compatible with JEDEC Standard AT27C4096**
- **Low Power CMOS Operation**
  - **20 µA max. (less than 1 µA typical) Standby for V_{CC} = 3.6V**
  - **36 mW max. Active at 5 MHz for V_{CC} = 3.6V**
- **JEDEC Standard Surface Mount Packages**
  - **44-Lead PLCC**
  - **40-Lead TSOP (10 x 14mm)**
- **High Reliability CMOS Technology**
  - **2,000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid™ Programming algorithm - 100 µs/word (typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
  - **JEDEC Standard for LVTTL and LVBO**
- **Integrated Product Identification Code**
- **Commercial and Industrial Temperature Ranges**

4-Megabit (256K x 16) Unregulated *Battery-Voltage*™ High-Speed OTP EPROM

AT27BV4096

Description

The AT27BV4096 is a high performance, low power, low voltage 4,194,304-bit one-time programmable read only memory (OTP EPROM) organized as 256K by 16 bits. It requires only one supply in the range of 2.7V to 3.6V in normal read mode operation. The by-16 organization makes this part ideal for portable and handheld 16 and 32 bit microprocessor based systems using either regulated or unregulated battery power.

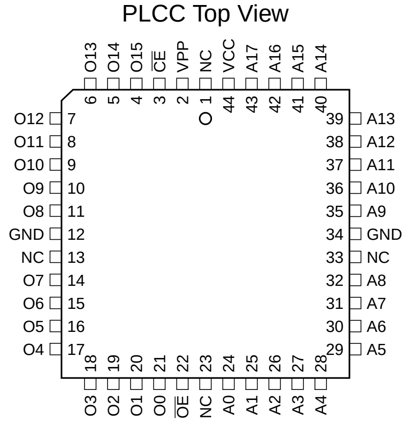
(continued)

Pin Configurations

Pin Name	Function
A0 - A17	Addresses
O0 - O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Connect

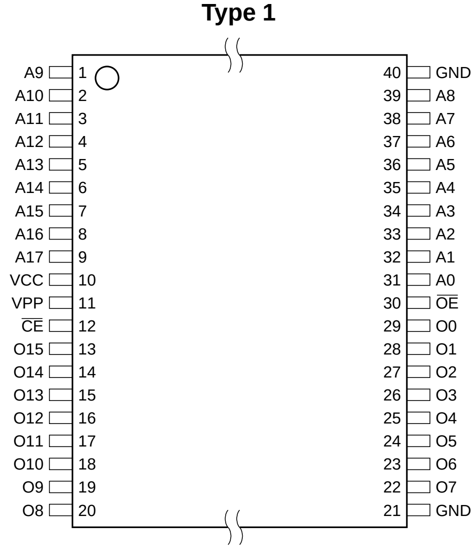
Note: Both GND pins must be connected.

PLCC Top View



Note: PLCC package pins 1 and 23 are DON'T CONNECT.

TSOP Top View
Type 1



Rev. 0640B–10/98

Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At V_{CC} = 2.7V, any word can be accessed in less than 120 ns. With a typical power dissipation of only 18 mW at 5 MHz and V_{CC} = 3V, the AT27BV4096 consumes less than one fifth the power of a standard 5V EPROM.

Standby mode supply current is typically less than 1 µA at 3V. The AT27BV4096 simplifies system design and stretches battery lifetime even further by eliminating the need for power supply regulation.

The AT27BV4096 is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

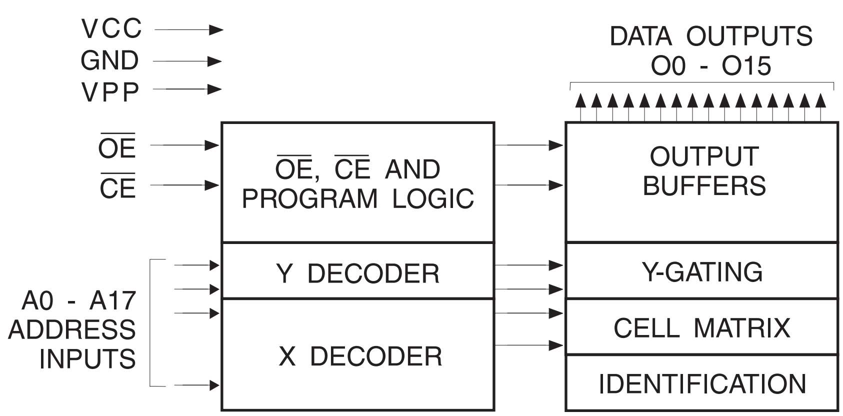
The AT27BV4096 operating with V_{CC} at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at V_{CC} = 5.0V. At V_{CC} = 2.7V, the part is compatible with JEDEC approved low voltage battery operation (LVBO) interface specifications. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

Atmel's AT27BV4096 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27BV4096 programs exactly the same way as a standard 5V AT27C4096 and uses the same programming equipment.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	V_{CC}	Outputs
Read(2)	V_{IL}	V_{IL}	Ai	X(1)	V_{CC}(2)	D_{OUT}
Output Disable(2)	X	V_{IH}	X	X	V_{CC}(2)	High Z
Standby(2)	V_{IH}	X	X	X (5)	V_{CC}(2)	High Z
Rapid Program(3)	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}(3)	D_{IN}
PGM Verify(3)	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}(3)	D_{OUT}
PGM Inhibit(3)	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}(3)	High Z
Product Identification(3)(5)	V_{IL}	V_{IL}	A9 = V_H(4) A0 = V_{IH} or V_{IL} A1 - A17 = V_{IL}	V_{CC}	V_{CC}(3)	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.

2. Read, output disable, and standby modes require, 2.7V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
4. V_H = 12.0 ± 0.5V.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27BV4096-12	AT27BV4096-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		2.7V to 3.6V	2.7V to 3.6V
		5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 2.7V to 3.6V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1}(2)	V_{PP}(1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC}(1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = $V_{CC} \pm$ 0.3V		20	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		100	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}, V_{CC} = 3.6V		10	mA
V_{IL}	Input Low Voltage	V_{CC} = 3.0 to 3.6V	-0.6	0.8	V
		V_{CC} = 2.7 to 3.6V	-0.6	0.2 x V_{CC}	V
V_{IH}	Input High Voltage	V_{CC} = 3.0 to 3.6V	2.0	V_{CC} + 0.5	V
		V_{CC} = 2.7 to 3.6V	0.7 x V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.4	V
		I_{OL} = 100 µA		0.2	V
		I_{OL} = 20 µA		0.1	V
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		V
		I_{OH} = -100 µA	V_{CC} - 0.2		V
		I_{OH} = -20 µA	V_{CC} - 0.1		V
V_{CC} = 4.5V to 5.5V					
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		±1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		±5	µA
I_{PP1}(2)	V_{PP}(1) Read/Standby Current	V_{PP} = V_{CC}		10	µA
I_{SB}	V_{CC}(1) Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		40	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

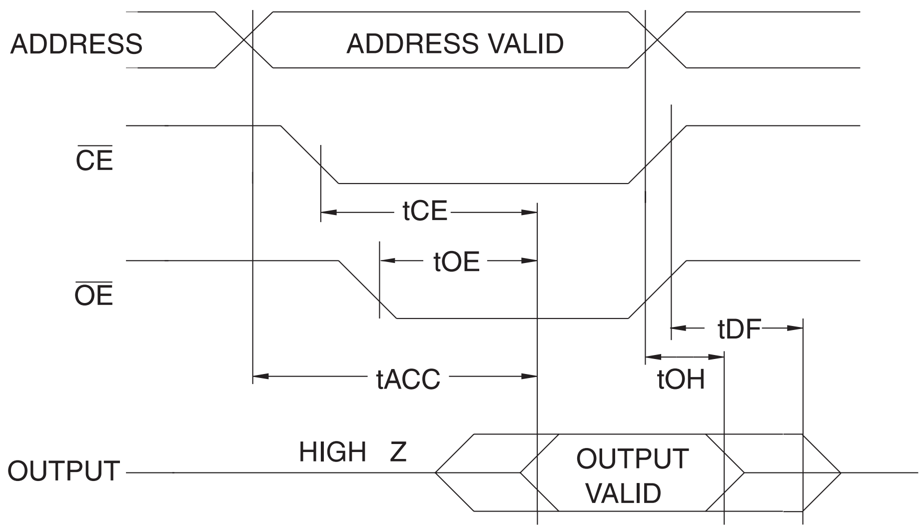
Notes:
1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}

AC Characteristics for Read Operation

V_{CC} = 2.7V to 3.6V and 4.5V to 5.5V

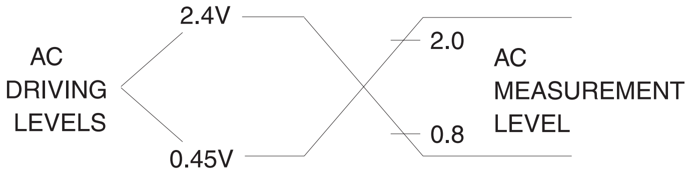
Symbol	Parameter	Condition	AT27BV4096-12		AT27BV4096-15		Units
			Min	Max	Min	Max	
t_{ACC}(3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		120		150	ns
t_{CE}(2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		120		150	ns
t_{OE}(2)(3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		35		50	ns
t_{DF}(4)(5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			30		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		ns

AC Waveforms for Read Operation(1)



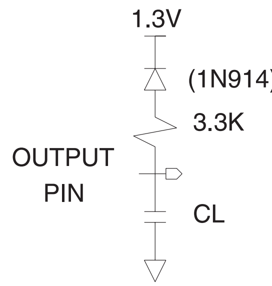
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.
6. When reading a 27BV4096, a 0.1 µF capacitor is required across V_{CC} and ground to suppress spurious voltage transients.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



Note: CL = 100 pF including jig capacitance.

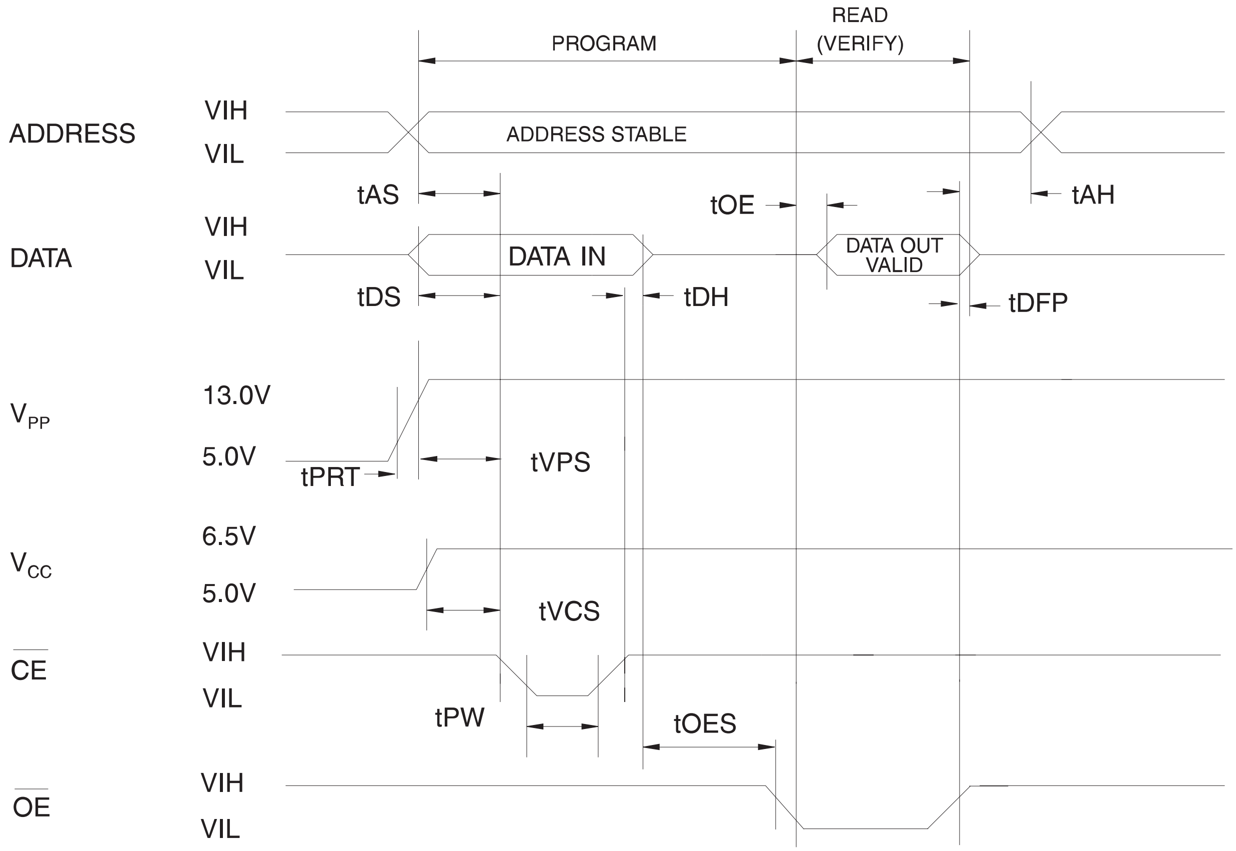
Pin Capacitance

f = 1 MHz T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms[1]



Notes: 1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27BV4096 a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

TA = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	mA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

TA = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions[1]	Limits		Units
			Min	Max	
t_{AS}	Address Setup Time	Input Rise and Fall Times: (10% to 90%) 20 ns Input Pulse Levels: 0.45V to 2.4V Input Timing Reference Level: 0.8V to 2.0V Output Timing Reference Level: 0.8V to 2.0V	2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay[2]		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width[3]		47.5	52.5	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

3. Program Pulse width tolerance is 50 µsec ± 5%.

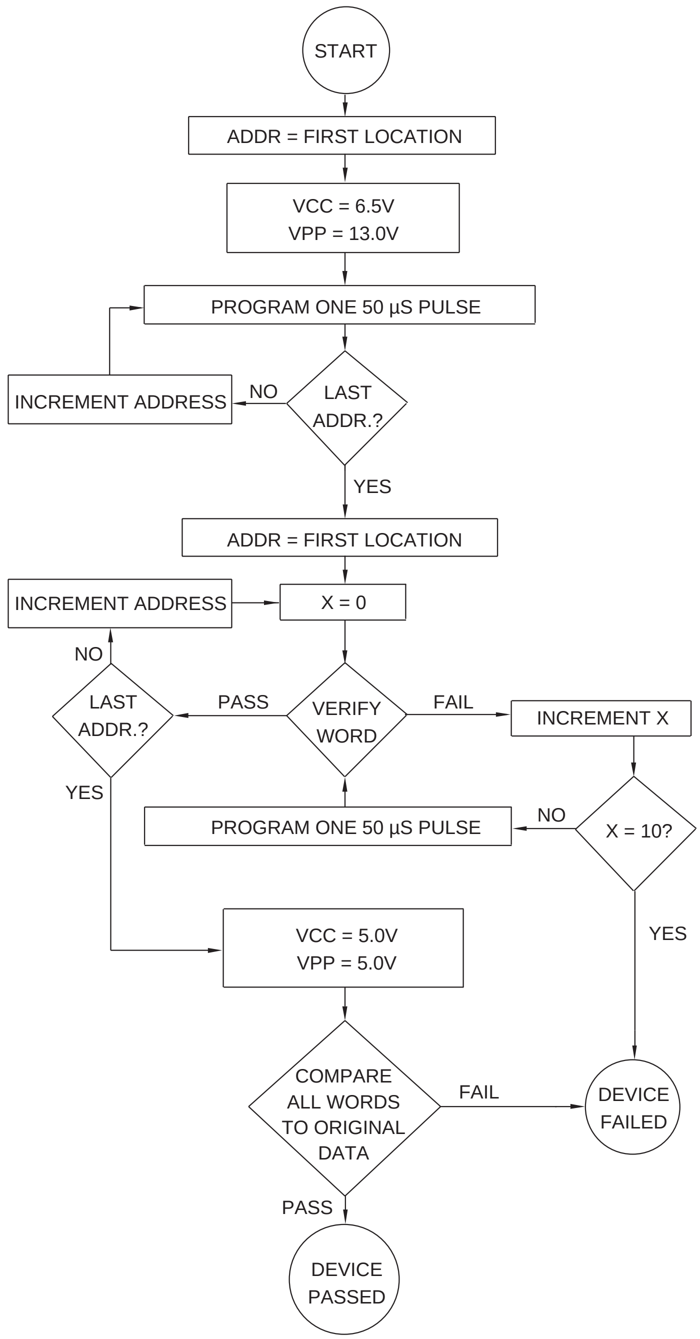
Atmel's 27BV4096 Integrated Product Identification Code[1]

Codes	Pins										Hex Data
	A0	O15-O8	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	1	0	0	00F4

Note: 1. The AT27BV4096 has the same Product Identification Code as the AT27C4096. Both are programming compatible.

Rapid Programming Algorithm

A 50 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 50 µs $\overline{CE}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.



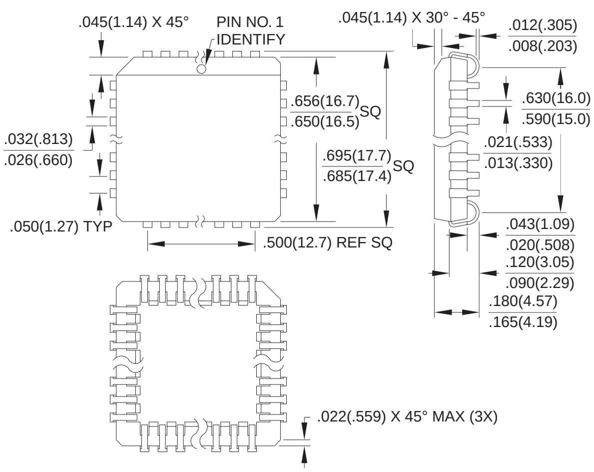
Ordering Information

t_{ACC} (ns)	I_{CC} (mA) Active	I_{CC} (mA) Standby	Ordering Code	Package	Operation Range
120	8	0.02	AT27BV4096-12JC AT27BV4096-12VC	44J 40V	Commercial (0°C to 70°C)
	8	0.02	AT27BV4096-12JI AT27BV4096-12VI	44J 40V	Industrial (-40°C to 85°C)
150	8	0.02	AT27BV4096-15JC AT27BV4096-15VC	44J 40V	Commercial (0°C to 70°C)
	8	0.02	AT27BV4096-15JI AT27BV4096-15VI	44J 40V	Industrial (-40°C to 85°C)

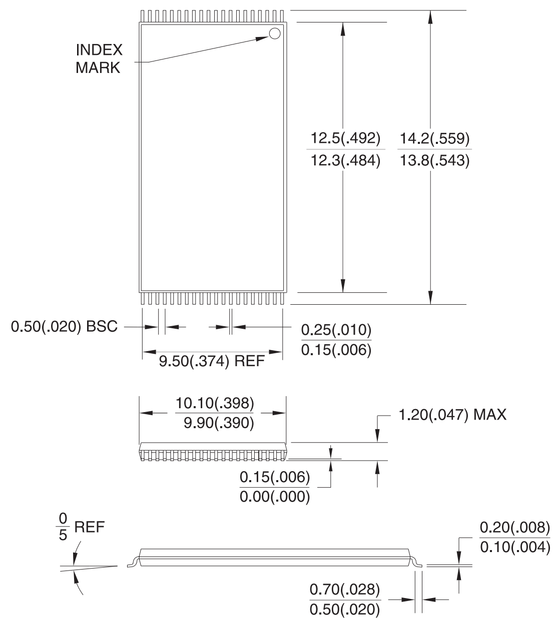
Package Type	
44J	44-Lead, Plastic J-Leaded Chip Carrier (PLCC)
40V	40-Lead, Plastic Thin Small Outline Package (TSOP) 10 x 14 mm

Packaging Information

44J, 44-Lead. Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



40V, 40-Lead. Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)
JEDEC OUTLINE MO-142 CA



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