Am27S18 • Am27S19

256-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 40ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

FUNCTIONAL DESCRIPTION

The Am27S18 and Am27S19 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 32 x 8 configuration, they are available in both open collector Am27S18 and three-state Am27S19 output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_4 and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to a logic HIGH, O_0-O_7 go to the off or high impedance state.

GENERIC SERIES CHARACTERISTICS

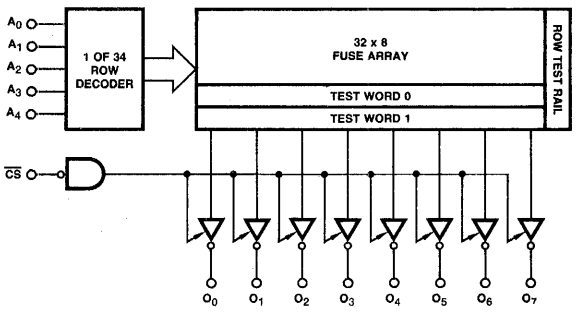
The Am27S18 and Am27S19 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large nonconductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

BLOCK DIAGRAM



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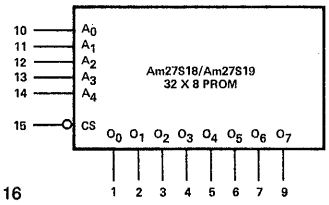
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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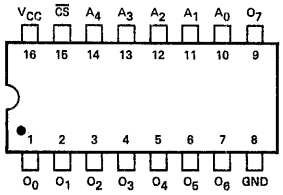
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM27S18DC
Hermetic DIP	−55°C to +125°C	AM27S18DM
Hermetic Flat Pak	−55°C to +125°C	AM27S18FM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM27S19DC
Hermetic DIP	−55°C to +125°C	AM27S19DM
Hermetic Flat Pak	−55°C to +125°C	AM27S19FM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to, +5mA

OPERATING RANGE

COM'L	Am27S18XC, Am27S19XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am27S18XM, Am27S19XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27LS19 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27LS19 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		90	115	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 4.5V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27LS19 only; V_O = 2.4V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am27LS19 only; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but periodically sampled.

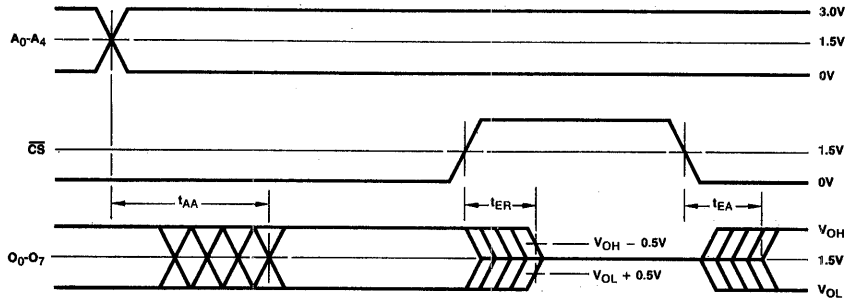
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	25	40	50	ns
t_{EA}	Enable Access Time		15	25	30	ns
t_{ER}	Enable Recovery Time		15	25	30	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

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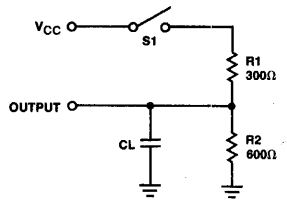
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

AC TEST LOAD



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PROGRAMMING

The Am27S18 and Am27S19 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

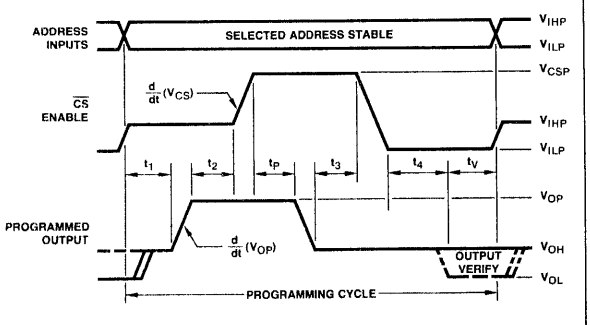
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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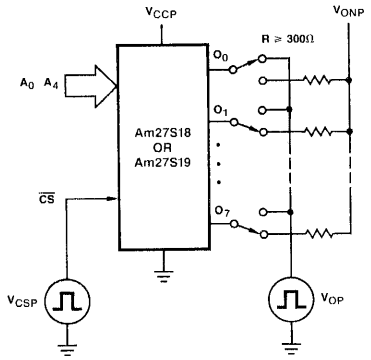
SIMPLIFIED PROGRAMMING DIAGRAM



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PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27S18 • Am27S19 ADAPTERS AND CONFIGURATOR	715-1407-1	PA16-6 and 32 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 32 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output O_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

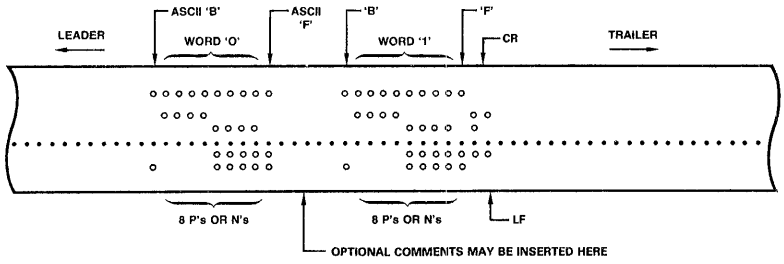
```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
Ø02   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
Ø04   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
Ø06   BPNNPPPNNF   HERE (R) (L)
 :    ::::::::::    :
Ø31   BNNNNPPPNF   END (R) (L)
```

(R) = CARRIAGE RETURN
(L) = LINE FEED

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ = LOW)

A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	H	H	L	H	L	L	H	H	H	L	L
		⋮						⋮				
H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



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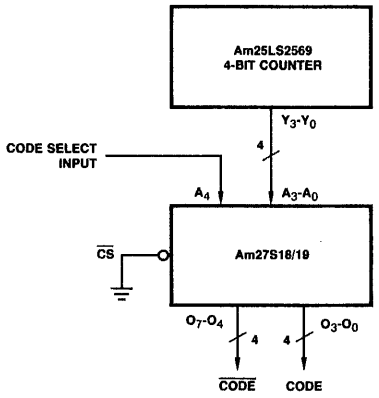
APPLYING THE Am27S18 AND Am27S19

The Am27S18 and Am27S19 PROMs may be used as code converters. Examples include conversion of hexadecimal, octal or BCD to seven segment display drive format. In many code conversion applications an extra PROM address input is available and may be used as a polarity control, blanking control or code selector input. The use of a single Am27S18 or Am27S19 to convert the outputs of a binary counter to either excess three or gray code format is illustrated below. In this case both codes are generated in true and complemented form simultaneously.



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TRUTH TABLE

ADDRESS					COMPLEMENT				TRUE				
A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	0	1	1	0	0	0	0	1	1	EXCESS THREE CODE
0	0	0	0	1	1	0	1	1	0	1	0	0	
0	0	0	1	0	1	0	1	0	0	1	0	1	
0	0	0	1	1	1	0	0	1	0	1	1	0	
0	0	1	0	0	1	0	0	0	0	1	1	1	
0	0	1	0	1	0	1	1	1	1	0	0	0	
0	0	1	1	0	0	1	1	0	1	0	0	1	
0	0	1	1	1	0	1	0	1	1	0	1	0	
0	1	0	0	0	0	1	0	0	1	0	1	1	
0	1	0	0	1	0	0	1	1	1	1	0	0	
0	1	0	1	0	X	X	X	X	X	X	X	X	
0	1	0	1	1	X	X	X	X	X	X	X	X	
0	1	1	0	0	X	X	X	X	X	X	X	X	
0	1	1	0	1	X	X	X	X	X	X	X	X	
0	1	1	1	0	X	X	X	X	X	X	X	X	
0	1	1	1	1	X	X	X	X	X	X	X	X	
1	0	0	0	0	1	1	1	1	0	0	0	0	GRAY CODE
1	0	0	0	1	1	1	1	0	0	0	0	1	
1	0	0	1	0	1	1	0	0	0	0	1	1	
1	0	0	1	1	1	1	0	1	0	0	1	0	
1	0	1	0	0	1	0	0	1	0	1	1	0	
1	0	1	0	1	1	0	0	0	0	1	1	1	
1	0	1	1	0	1	0	1	0	0	1	0	1	
1	0	1	1	1	1	0	1	1	0	1	0	0	
1	1	0	0	0	0	0	1	1	1	1	0	0	
1	1	0	0	1	0	0	1	0	1	1	0	1	
1	1	0	1	0	0	0	0	0	1	1	1	1	
1	1	0	1	1	0	0	0	1	1	1	1	0	
1	1	1	0	0	0	1	0	1	1	0	1	0	
1	1	1	0	1	0	1	0	0	1	0	1	1	
1	1	1	1	0	0	1	1	0	1	0	0	1	
1	1	1	1	1	0	1	1	1	1	0	0	0	